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FINAL REPORT

DESIGN AND FABRICATION OF A CCD CAMERA FOR USE WITH RELAY OPTICS IN SOLAR X-RAY ASTRONOMY

CONTRACT NASW-3784

PREPARED FOR:
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
WASHINGTON, D.C. 205466

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DESIGN AND FABRICATION OF A CCD CAMERA FOR USE WITH RELAY OPTICS IN SOLAR X-RAY ASTRONOMY

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Prepared by: American Science and Engineering, Inc.
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Prepared for: National Aeronautics and Space Administration
Washington, D.C. 20546

Period of Performance: 1 July 1983 to 30 September 1984

Approved by: John M. Davis

John M. Davis
Director of Space Research

FOREWORD

To acquire solar X-ray images from a remote spacecraft, it is necessary to record the images in such a way that they can be transmitted digitally to the earth. This requires the development of a camera consisting of an X-ray sensitive detector and the electronics to process and transmit the image data. The object of Contract NASW-3784 was to design and fabricate such a camera based on an RCA CCD chip. This effort has been successful and the resulting design is described in this report.

The design and development of the CCD camera has been the responsibility of Raymond Counterman, working under the direction of Dr. John M. Davis, the Principal Investigator. Their starting point was the preliminary design made for a CCD X-ray camera for the CXX (Coronagraph X-Ray XUV) telescope for ISPM (International Solar Polar Mission). This earlier work was performed under subcontract S-9003 to the National Center for Atmospheric Research (NCAR). Daniel O'Mara assisted in the testing of the CCD, particularly in the operation of the vacuum and cooling systems and in the use of the visible light and X-ray sources.

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1.0 INTRODUCTION

Our understanding of the physical conditions existing in the solar corona has increased rapidly during the past decade. This is a result of our ability to view the spatial structures of the corona at high resolution in soft X-rays. The subsequent visual identification of a diverse population of coronal structures has provided both a new framework for the reformulation of the more classical concepts of solar physics and an incentive for new ideas.

X-ray images provide essential information not only on the physical size, spatial coherency and location with respect to other features, of the coronal structures but also, through the use of filter techniques, on various plasma diagnostics, e.g., temperature, emission measure, pressure, density. These diagnostics describe the general properties of the plasma because they are averaged over many wavelengths. However, their unique advantage is that they provide simultaneous observations over a complete structure.

In the past decade the emphasis has been placed on obtaining observations with the highest spatial resolution, which has meant using photographic film as the recording medium. Film has several disadvantages; it has a low sensitivity, which translates into poor temporal resolution, is difficult to calibrate, and must be recovered. To overcome these limitations, various electronic imaging systems have been proposed. In general these systems are characterized by very high sensitivity ($\sim 10^3 - 10^4$) but rather poor spatial resolution ($\sim 1/10$) when compared to film.

Among the most promising devices for this application are CCDs which are closely spaced, two-dimensional arrays, of MOS capacitors laid down on a silicon substrate. The capacitors are electrically isolated from each other by the p- and n-type architecture of the device and by the applied voltages. A photosite, or picture element (pixel), consists of a set of three adjacent capacitors grouped in the columns of the array. The electrodes of the capacitors are independently controlled by "clock" or "gate" voltages. Because of this arrangement this type of CCD is known as a three-phase device.

When an incident X-ray is absorbed in the silicon substrate it excites electrons into the conduction band which then diffuse into a depletion layer formed by the positive voltages applied to the electrodes. These applied voltages form a potential well which traps charge at a particular photosite. To read out the device the applied voltages are changed, or clocked, so that the charge at each photosite along a row is transferred vertically to the adjacent site in its column. The charges in the row formed by the lowest site in each column are transferred into a shift register where they are read out serially following on-chip amplification.

The key to the operation of the CCD as an X-ray detector is the use of the interaction site as the storage site. It can be thought of as an array of solid state detectors each with its own memory for the CCD can accept photons over its entire surface simultaneously.

In conventional X-ray detection, the detector is used exactly as for visible light detection, as a total energy detector. The output of a particular pixel is a charge which is proportional to the total amount of energy deposited in the pixel. The spatial resolution is determined largely on the basis of pixel-to-pixel spacing and charge localization between pixels.

On the average one electron-hole pair is created in the pixel for every 3.6 eV of energy in the X-ray photon. This is a very small amount of energy when compared with other soft X-ray detectors. Thus, a proportionally greater number of electrons will be created for each photon interaction, and the associated Poisson (or Poisson-like) statistics become more precise.

CCDs have several important characteristics which influence their operation as X-ray imaging detectors. First is the quantum efficiency, defined as the probability of detecting an incident photon. It is a function of X-ray energy and is close to unity for energies between 1 and 10 kilovolts. At the higher energies the efficiency falls off because the photons pass through the device without interacting while at the low energies the X-ray photons are absorbed by the electrode and insulating structures on the front surface. These structures form a dead layer between 0.5 and 2 microns thick, and to overcome their effect CCDs have been operated in a back-illuminated mode. In this case the silicon

substrate is illuminated directly, and to maximize the efficiency its thickness is tailored to the particular application, a process known as thinning.

The intrinsic noise of a CCD limits the length of time a picture can be integrated. Noise levels of 30 electrons rms can be achieved corresponding to energy resolution of 250 eV. The energy resolution is essentially independent of energy, and therefore CCDs are better than proportional counters at energies above 500 eV and marginally worse at lower energies. The ultimate noise goal is order of 10 electrons rms, which would be set by the stray capacitance of a few hundred pFs between the on-chip preamplifier and the last transfer gate.

To achieve these noise levels, the CCD and the on-chip amplifier have been cooled. Typical operating temperatures are around -100°C. However, if the operating temperature is made too low, the charge transfer efficiency falls off. The charge transfer efficiency is the fraction of the original charge transferred from one pixel to the next during the readout process. Incomplete charge transfer results in a loss of both photometric accuracy and dynamic range and introduces smearing of the image. In our tests with RCA CCDs we have found that an ideal operating temperature must be determined, for each device. It must be warm enough so that charge transfer efficiency is adequate (0.99995 to 0.99999) while still cool enough to keep the leakage current acceptably low. The leakage current is a measure of the charge that spills from an illuminated pixel to adjacent dark pixels.

In principle the dynamic range of the CCD is limited by the read-out noise and the full well capacity. The latter scales roughly as the pixel area, and for 30 micron square pixels the well capacity is 250,000 electrons. The typical dc level for the three-phase CCDs we have tested is several hundred electrons, which corresponds to a dynamic range of the order of or less than 10^3.

Although one should be able to extend the dynamic range by improving the noise characteristics of the preamplifier this is not necessarily true in the X-ray region. For a single X-ray photon produces a large number of electrons, e.g., a one kilovolt X-ray will contribute in excess of 300 electrons, and if this value is greater than the noise it will place the limit on the dynamic range

which is thus energy dependent varying inversely with the incident photon energy.

Finally, CCDs have the excellent linearity to increases in the incident X-ray intensity, a characteristic of solid state detectors. Pixel non-uniformities arising from processing variations and mask alignment errors during fabrication are generally quite small.

CCDs from several manufacturers have been tested at AS&E but only RCA, back-illuminated chips, of the SID 500 series have proved capable of detecting X-rays in the 250 eV energy range (44 A). Consequently, a device of this type is used in our camera design.

2.0 THE CCD CAMERA

2.1 General System Description

The Camera System, which is configured as a subsystem of a sounding rocket experiment, is used to record and transmit an X-ray image focused on a Charge-Coupled Device (CCD). The components of the system are: the shutters and filters, the experiment computer, the telemetry interface, and the CCD camera. The relationship between these components is shown in the Camera System Block Diagram (Figure 1).

The experiment computer operates the electromechanical systems and the CCD Camera in the sounding rocket experiment. Specifically to the Camera System, it operates the shutters and filters which are located in the optical path just before the CCD focal plane and selects a preprogramed picture sequence for the camera. The computer also decides when to take a picture during the experiment, which filter to use, which determines the bandpass of the image, and the exposure period.

When the CCD is read out, the camera formats the digital picture data and passes it to the telemetry interface from where it is transmitted to the ground. In order to ensure the synchronization of the telemetry frame and the CCD image readout clock signals generated in the telemetry system are passed to the camera electronics.

The camera converts the X-Ray image focussed on the CCD into a 256 by 256 pixel array with each pixel magnitude represented by a digital word. The camera is physically divided into two parts, the CCD Head Electronics package and the Camera Electronics package. The CCD detector, located in the CCD Head Electronics package, is a Charge-Coupled Device thinned and back illuminated for X-Ray imaging (RCA SID 53634-X0). This package also contains a preamplifier for the CCD video output, level shifting of the logic-level clock signals, and associated reference voltages.

CAMERA SYSTEM BLOCK DIAGRAM

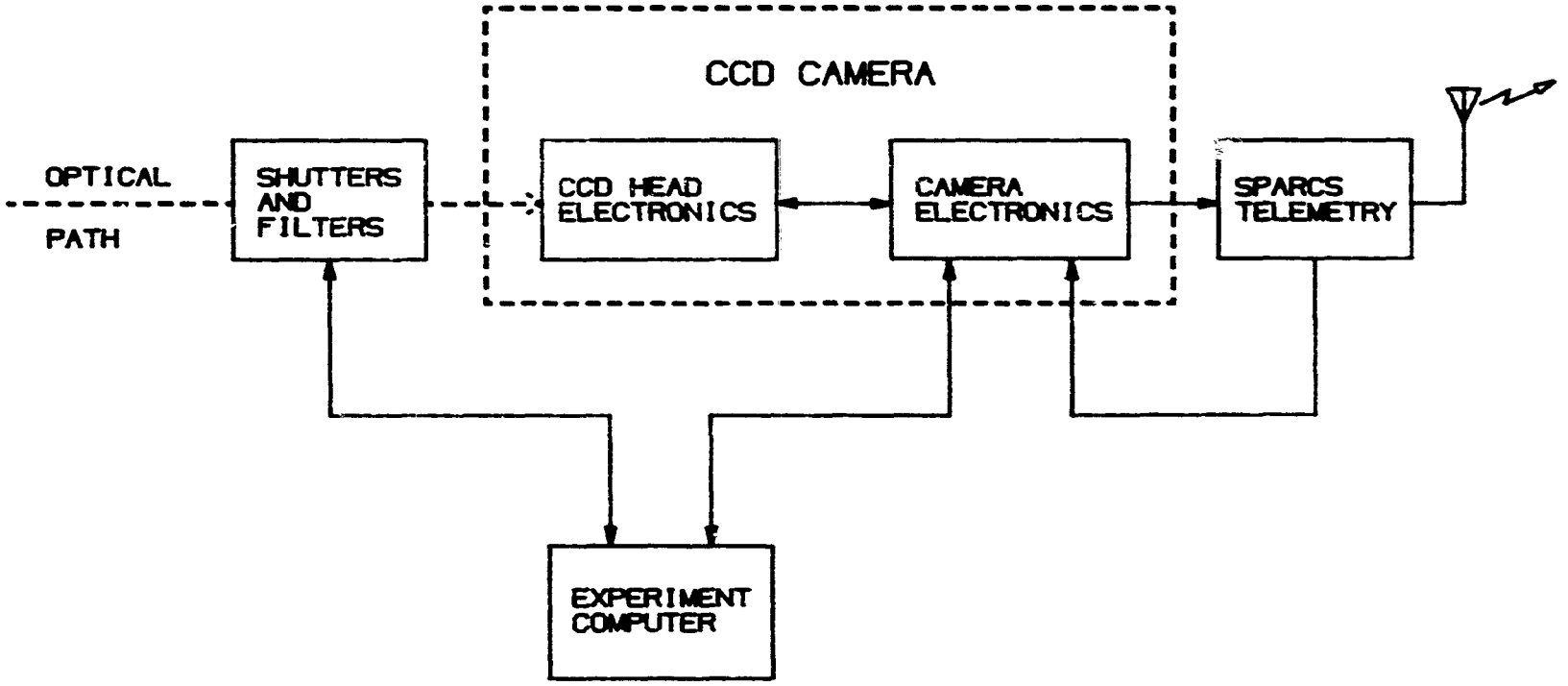


Figure 1

The Camera Electronics package contains the circuitry for processing the analog signal from the CCD Head Electronics package, for generating CCD clock waveforms, and for interfacing with telemetry and the Experiment Computer.

2.2 General System Operation

The CCD Camera has been designed as part of a sounding rocket experiment for studying solar X-Rays. During the flight the Camera System is powered at the beginning of the experiment period. The sequence of experiment events is stored in the memory of an on board computer called the Experiment Computer. It is this computer that controls the shutter and filter electromechanical systems and the CCD Camera. At selected periods during the experiment the CCD Camera is used to take X-Ray images of the sun via an X-Ray telescope.

Once the CCD Camera is powered it begins what is called an erase routine. The erase routine, stored in a microcontroller in the camera, continually removes charge from the image and storage areas of the CCD providing a clean slate, so to speak, on which a picture can be imaged. This charge is the result of thermal noise which accumulates in the potential wells of the CCD and is a function of the CCDs temperature. Therefore the CCD, when used as a slow scanned device, which it must be in this application since it takes several seconds to transfer the picture data to telemetry has to be cooled. The operating temperature determined experimentally is $-80 \pm 20°C$.

Upon a command from the Experiment Computer the camera completes the current erase routine leaving the image area of the CCD ready for an exposure. At this point, the camera sends a command to the Experiment Computer to begin the exposure. The computer operates the shutters to expose the CCD to X-Rays for a period programed in it's memory. Then, commanded by the Experiment Computer, the CCD Camera reads out the image from the CCD and converts the analog signal into a digital word. The Camera formats the pixel intensity data, pixel number, filter type, and exposure period into the telemetry frame using synchronization signals from the telemetry clock. In this manner sequences of X-Ray images are transmitted to the ground station where the data is recorded and displayed in real time monitoring. A typical sequence consists of three exposures differing in time by a factor of 3 through each of 2 different filters.

At the end of the experiment the Camera System is powered down for re-entry of the payload.

2.3 System Features

The CCD Camera has been designed with the following key features:

- o Programmable Clock Generator Waveforms
- o Adjustable Raster Width/Position
- o Selectable Camera Mode of Operation
- o Correlated Double Sample and Hold with adjustable Black Level Offset
- o Programmable CCD Operations
- o Programmable Telemetry Frame Formatting
- o Externally Controlled Exposure

which are described in detail below.

2.3.1 Programmable Clock Generator Waveforms

The camera is designed around a three phase charge coupled image sensor and is easily modified to meet new system criteria. The CCD clock signals, correlated double sample and hold timing signals, and the analog to digital conversion timing signals are generated by reading an EPROM. The EPROM's UV erasable memory stores the ones and zeros that generate each signal and can be reprogrammed to optimize the operation of the CCD selected, the sampled and hold circuit, and the ADC circuit.

2.3.2 Adjustable Raster Width/Position

The CCD device has an image area of 320 horizontal by 256 vertical pixels. The camera outputs an array of 256 vertical lines and has an adjustable width/position feature for the horizontal line. This adjustment is on the Raster Limit Board where there are wired circuits, jumpers, used to define the location of the first and last pixel of a horizontal line in the CCD output array. Therefore the image array horizontal dimensions are flexible and can be changed by

moving jumpers on the board. The width used in the current design is 256 pixels and their position is selected to use the area of the CCD with the fewest blemishes.

2.3.3 Selectable Camera Mode of Operation

The camera has two modes of operation called the "Data Output Mode" and the "Telemetry Output Mode". The default mode is the telemetry output mode, used in the flight. The Data Output Mode, used for test, allows the image to be read at the clock pixel rate of 52 microseconds. A data valid pulse is generated for loading the data into an external imaging system. This signal and the pixel data signals are wired to a connector labeled "Data Output".

The Telemetry Output Mode allows the clock generator to be synchronized to the Telemetry system. The telemetry interface is via a connector labeled "Telemetry Output". Mode selection is accomplished by sending a logic level signal to a pin on the Experiment Computer connector. A logic one selects the Data Output Mode and a logic zero or no signal present selects the Telemetry Output Mode.

2.3.4 Correlated Double Sample and Hold with Adjustable Black Level Offset

The function of the correlated double sample and hold (S/H) is to generate a voltage proportional to the difference between the pixel charge level and the background level. This provides the magnitude of the pixel charge due to the photon source. The background level or black level has an adjustable DC component so that the black level can be set to zero volts, i.e. no image results in a S/H output of zero volts. This adjustment also allows any offsets in the preamplifier to be nulled out.

2.3.5 Programmable CCD Operations

The Clock Generator circuitry moves charge in the CCD by four commands; Image Transfer (IT), Line Transfer (LT), Line Read (LR), and Pixel Read (PR). The Image Transfer command moves the entire image from the image area of the CCD to the storage area. The Line Transfer command moves one line of charge from the storage area to the horizontal readout register. The Line Read command, in the

Data Output Mode, reads the entire horizontal register converting pixel charge into digital data. The Pixel Read command, in the Telemetry Output Mode, reads out only pixels in the horizontal line which are to be converted and reads one pixel per command signal. Those pixels which are not converted in the line are dumped by the Line Read command when in the Telemetry Output Mode of the camera operation.

The program of transfer and read operations described above is stored in the EPROM of the Camera Microcontroller. This allows flexibility in modifying the camera to vary such processes as the erasure of the CCD image area.

2.3.6 Programmable Telemetry Frame Formatting

The CCD Clock Generator is synchronized to telemetry by a microcontroller. This programmable controller formats pixel data, experiment computer data and internal microcontroller generated data into a 32-word frame suitable for transmission via telemetry. The type of data and location of the data word in the frame can be changed by reprogramming the Telemetry Microcontroller.

2.3.7 Externally Controlled Exposure

The control of the CCD exposure is external to the camera which allows the exposure period of each picture to be stored in the memory of the Experiment Computer. The Experiment Computer also controls the shutters and filters and the sequential timing of the picture taking events.

During times when a picture is not being taken, the image area of the CCD is continually erased of thermal charge. To record an image the Experiment Computer informs the camera that it would like to take a picture, i.e., begin exposing the CCD. The camera completes the current erase routine and prepares the image area for exposure. When this is done it informs the Experiment Computer to begin the exposure. After completion of the exposure, the camera is signaled to read out the image.

3.0 SUBSYSTEM MODULE DESCRIPTION

Physically the Camera System has been subdivided into seven functional blocks or modules. The two modules of the CCD Head Electronics Package are the CCD Head Electronics Module and the CCD Image Sensor. In the Camera Electronics Package there are five modules which are: the Clock Generator, Camera Microcontroller, the Correlated Double Sample and Hold, the ADC, and the Telemetry Interface.

The CCD Head Electronics Module consists of a single printed circuit board which is mounted close to the CCD Image Sensor. There are twenty-four wires to connect the Image Sensor to the CCD Head Electronics Module. The CCD Head Electronics Module is connected to the Camera Electronics Package via a cable.

The modules of the Camera Electronics Package are mounted in a card cage enclosure which allows their interconnection to be made on a backplane. This package interfaces to other system components via cables and D-type connectors.

3.1 Modules of the CCD Head Electronics Package

3.1.1 The CCD Head Electronics Module

Figure 2, the CCD Camera Block Diagram, illustrates the basic signal paths for the modular view of the camera. The CCD Head Electronics Module contains a video preamplifier, an active load for the CCD output transistor, level shifters, and voltage references. The CCD output signal is buffered by the preamplifier providing a low impedance source for the correlated double sample and hold circuit in the following stage. This preamplifier has a gain of 13. The active load is a current sink for the CCD output transistor which increases the output level and thereby the improves the characteristics of the CCD output stage. The signals from the CCD Clock Generator Module enter the Camera Head at either a 0 or a +5 volt logical level. The clock levels required by the CCD Image Sensor are at various analog levels and not at these logic levels. The translation is accomplished on the CCD Head Electronics board by using a reference voltage for the CCD analog level and shifting the input signal to this

CCD CAMERA BLOCK DIAGRAM

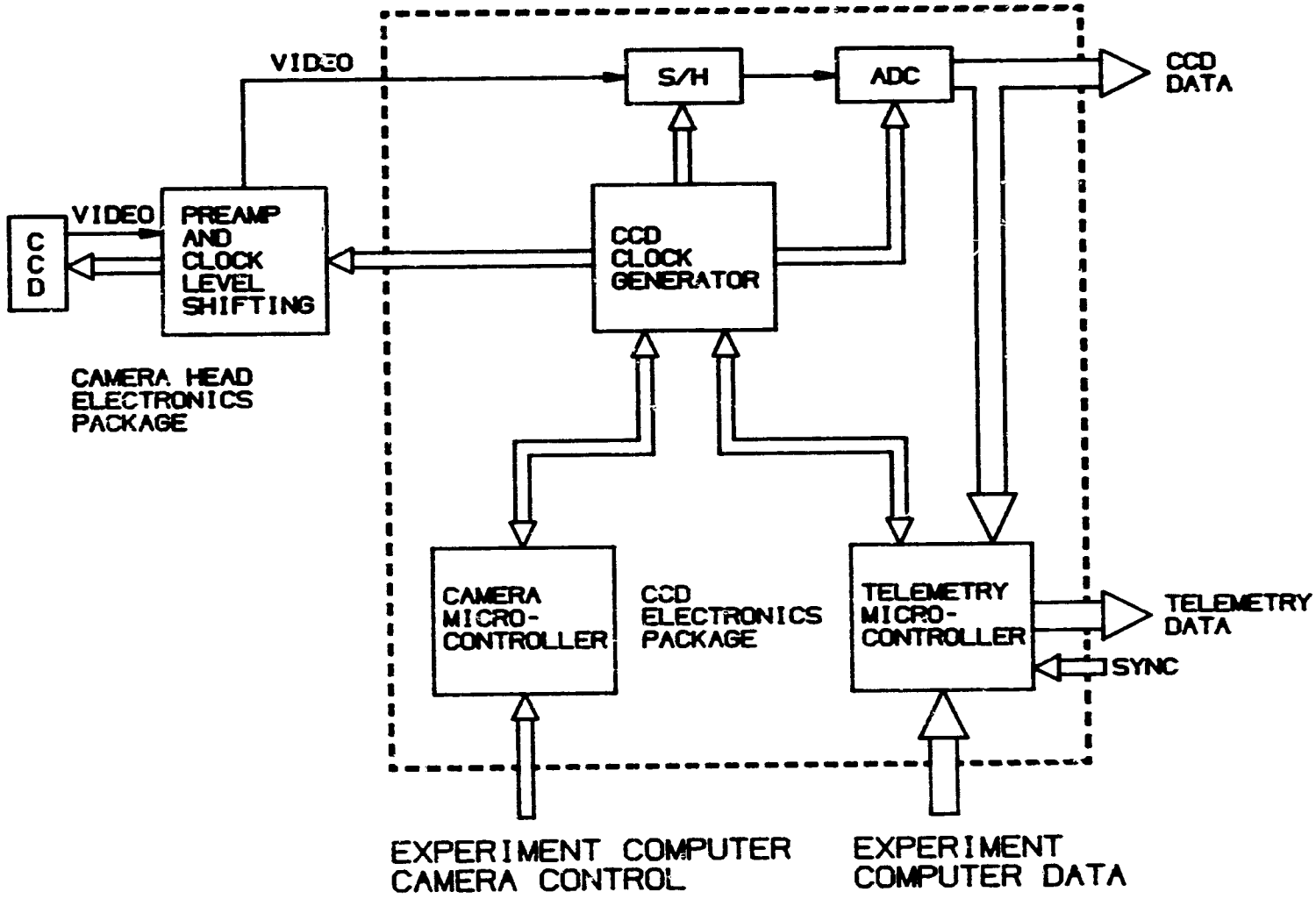


Figure 2

level. This also isolates the digital control circuitry from the CCD analog circuits.

3.2 CCD Image Sensor

The CCD Camera used an RCA SID 53634-X0 sensor which is intended primarily for use in generating standard interlaced 525-line television pictures. This device utilizes an array of charge coupled device (CCD) shift registers for photo-sensing and readout. It contains 512 vertical x 320 horizontal pixels (163,840 picture elements). The device is constructed with a 3-phase, N-channel, Vertical Frame Transfer organization using a sealed silicon gate structure. The device features high resolution combined with ultra-low blooming characteristics. Overall picture performance is comparable to that of 2/3-inch vidicon camera tubes but undesirable characteristics such as lag and microphonics are eliminated. For use in the X-ray region the device is thinned and back illuminated. The sensitivity of the device to X-rays in the range 8-44 A has been verified experimentally during this program.

3.2.1 Image Area

The image area is an array of analog buried channel CCD shift registers containing 320 parallel vertical columns of 256 sensing cells. An elemental cell is defined by a grouping of three adjacent polysilicon gate electrodes in the vertical direction and adjacent channel stops in the horizontal direction. The three gates in each cell are connected in parallel with the corresponding gates in he other cells. These three connections are called vertical clocks VA1, VA2, and VA3.

The transfer electrodes are made of polysilicon which is not transparent to soft X-rays. The device used in the X-ray camera has been altered by creating a window in the ceramic substrate. This allows illumination of CCDs backside. The back illumination of the thinned CCD sensor provides the camera with X-ray sensitivity.

3.2.2 Storage Area

The storage area has the same construction as the image area and also contains 320 parallel vertical columns of 256 sensing cells which line up the image area columns. This area serves as a temporary storage site for the previous TV picture field to allow conversation of the charge pattern image into a sequential horizontal readout. The storage area must normally be covered by an external light shield.

There are three storage area clock drivers, VB1, VB2 and VB3. The storage area is clocked in unison with the image area to transfer the complete image from the image area to the storage area.

3.2.3 Horizontal Register

The output register has the same 3 phase operation as the image and storage areas. The clock drives are VH1, VH2, and VH3. This register is fabricated with buried channel construction for maximum transfer efficiency during the high speed readout. This insures uniformly high resolution in all parts of the picture.

The horizontal register receives one line of picture information from the storage area. The register contains 320 cells corresponding to each of the 320 columns in the image and storage areas plus two additional cells at the output. Typically, in a television application, the register is "over-clocked" by several pulses to provide a clean dark signal for video black level clamping at the end of a line. For the CCD camera application, each pixel is referenced to black by the correlated double sample and hold circuit. The horizontal register is overclocked (332 shifts of the register) ensuring a clean register for the next line of the image. The signal is extracted by the output circuit.

3.2.4 Output Circuit

The CCD signal is extracted from the horizontal register by the circuit shown below (Figure 3). OG is the last CCD gate in the horizontal register. The CCD signal charge is collected at the floating diffusion gate. This gate is reset to a positive potential once each clock cycle by VD and VR. The voltage change on the floating diffusion gate is the signal which is sensed by the output transistor. The signal is taken from OS as a source follower shown here with a resistive load. An active load is used in the CCD camera design to provide a higher output level (see Circuit Diagram 652-4107).

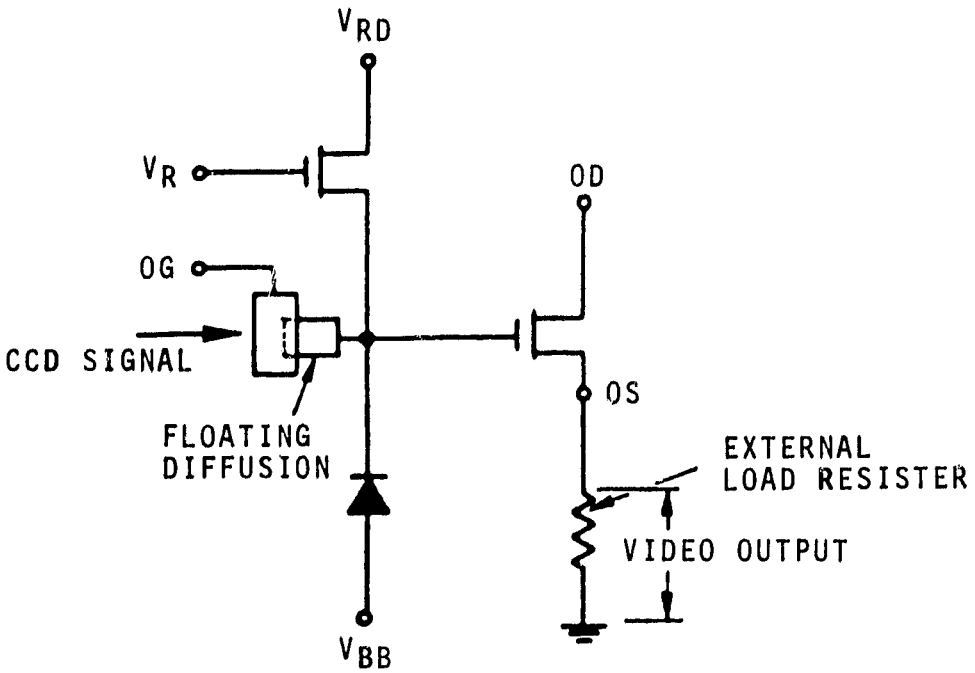


Figure 3. Output Circuit

3.3 Modules of the Camera Electronics Package

3.3.1 The Clock Generator Module

The Clock Generator provides the CCD with waveforms that perform charge moving operations in the device. It also provides the timing signals for converting the CCD analog output into digital data. The module is controlled by both the Camera and Telemetry microcontrollers.

There are ten CCD clocking signals from this module to the Camera Head Electronics Package. Four are used to read the horizontal register (VR, VH1, VH2, VH3), three to shift lines of charge in the image area (VA1, VA2, VA3), and three to shift lines of charge in the storage area (VB1, VB2, VB3). There are three signals for the Correlated Double Sample and Hold Module (CLAMPN, SAMPN, SUPRN). One signal goes to the ADC Module (CONVN). The five signals which interface the Clock Generator to the Camera Microcontroller are called: Image Transfer, Line Transfer, Line Read, Busy, and Enable ADC. Pixel Read and Convert Window interface the Clock Generator to the Telemetry Microcontroller.

The Clock Generator performs four charge-moving operations on the CCD. These are Image Transfer, Line Transfer, Line Read, and Pixel Read. The functioning of the Line Read and Pixel Read operations depend on which of the two camera modes of operation are selected either the Data Output Mode or the Telemetry Output Mode. The Telemetry Output Mode allows the Clock Generator to be synchronized to the telemetry system and the Data Output Mode allows a line of data to be read to an external imaging system at the internal pixel clock rate. These four operations are each intiated by a pulse to their respective Clock Generator input line (IT,LT,LR,PR).

A Line Transfer (LT) moves lines of charge in the storage area and a line from the storage area to the horizontal register. The storage area can be visualized as an matrix of 256 rows by 320 columns, S(i,j), and the horizontal register H(i) as a row under the last row of the storage area. The Line Transfer operation moves a row to the row below it. S(1,j) moves to S(2,j), S(2,j) moves to S(3,j) etc. The last row of the storage area S(256,j) is shifted into the horizontal register so that these charges can be shifted horizontally.

An Image Transfer (IT) is similar to the Line Transfer in that lines of charge are moved. The Image Transfer moves 256 lines of charge from the image area to the storage area. The image area can be thought of as a 256 by 320 matrix I(i,j). Again as in the Line Transfer I(1,j) moves to I(2,j), I(2,j) moves to I(3,j), etc. The bottom row of the image area I(256,j) is moved to the top row of the storage area S(1,j) and also S(1,j) moves to S(2,j), S(2,j) moves to S(3,j) and so forth. The Image Transfer operation moves the 256 rows of the image area to the 256 rows of the storage area. This transfers the picture from the image to the storage area.

The Horizontal Register is a row matrix of 320 pixels. The picture array which is imaged is only 256 pixels wide. This means that a section of the Horizontal Register contains 256 pixels to be digitized and a total of 64 pixels some before or after this section which are unused. For this explanation, let's assume the imaged pictured is centered on the CCD resulting in 32 unused pixels before the picture data and 32 pixels after the picture data in a line. The actual position of the picture array is adjustable within the Clock Generator Module as described earlier.

A Line Read operation shifts charge horizontally in the Horizontal Register to the CCD output transistor and converts 256 pixels into digital data. In the Data Output Mode the Camera is sending data to an external imaging system where the 256 pixels of the image are displayed at the internal pixel clock rate. The first 32 pixels of the line are shifted to the output transistor and no conversion is performed. The following 256 pixels are shifted one by one to the output transistor and after signal processing and conversion are sent to the external imaging system. The end of the line (last 32 pixels) is then read with no conversion.

The Line Read performs differently in the Telemetry Output Mode which synchronizes the picture readout to the telemetry system. In this mode the Pixel Read operation is valid. Upon a line read command from the Camera Microcontroller the Clock Generator reads the first 32 pixels of the current line in the Horizontal Register plus the first pixel of the picture array which is converted and output to the ADC Bus. The Telemetry Microcontroller then takes control of

the rest of the line readout. This controller loads the 33rd pixel into the a word of a frame and sends a Pixel Read command to the Clock Generator. This command shifts the next pixel into the CCD output transistor, converts the signal to digital data, and sends it to the ADC Bus where it can be loaded by the Telemetry Microcontroller into a frame. After the last pixel of the picture array H(256+32) is read into telemetry the Line Read command completes its operation by reading the 32 unused pixels at the end of the line. During a Line Read or Pixel Read operation a pixel charge is shifted to the CCD output transistor and amplified. The Clock Generator provides the timing signals to the Correlated Double Sample and Hold and the ADC circuits which convert the magnitude of the pixel charge due the X-Rays, which were imaged on that pixel, into an 8 bit word.

To summarize, the four operations of the Clock Generator Module in the Telemetry Output Mode are:

Image Transfer(IT) - Moves the image to the storage area.
Line Transfer(LT) - Vertically shifts a line of the storage area into the horizontal register.
Line Read(LR) - Reads out a line up to and including the first pixel to be converted and the end of a line after the last pixel is converted.
Pixel Read(PR) - Reads one pixel.

3.3.2 The Camera Microcontroller Module

The camera microcontroller module controls the Clock Generator and communicates with the flight Experiment Computer. It is responsible for the sequence of Image Transfer/Line Transfer/Line Read operations.

The module consists of one printed circuit board with seven I/O lines. Seven signals are used, five internal to the camera and two which interface with the Experiment Computer. Busy, Image Transfer, Line Transfer, and Line Read are signals to and from the Clock Generator. Enable ADC is an output used by the Clock Generator, ADC, and the Telemetry modules and specifies that a picture is

being read. Begin Picture Sequence/Transmit Picture and Expose Image Area /Transmission Complete are the two signals that communicate with the Experiment Computer.

The heart of the module is an Intel 8748 single chip 8-bit microcomputer with 1K bytes of erasable and programmable program memory and 64k bytes of RAM. The use of this device gives the camera a great deal of flexibility and allows different operating schemes to be accommodated easily.

The CCD support circuitry is involved in two activities. First, during dormant intervals when the camera is not imaging or transmitting the image area of CCD sensor must be kept clean of charge. This is called the Erase Routine. In the second, the camera interacts with the Experiment Computer to transmit a picture. This is called the Picture Routine.

An Image Transfer moves all the charge in the image area to the storage area and all the charge of the storage area to the Horizontal Register. The Horizontal Register is subsequently emptied of charge by the Line Read operation. The Erase Routine is composed of N repetitions of an image transfer operation followed by a Line Read operation. The Erase Routine must be capable of cleaning the charge that builds up in the image area during the reading and transmission of the picture that resides in the storage area. The magnitude of this charge is dependent on the CCD temperature and therefore also the number of cycles,N, required to remove the charge is also temperature dependent. N can be chosen experimentally, although it is desirable to have N as small as possible to keep processing time to a minimum.

The Experiment Computer initiates the Picture Routine by setting the signal Begin Picture Sequence/Transmit Picture to one. The Microcontroller then completes the current Erase Routine and leaves the image area ready for an exposure. Once this is done the Microcontroller informs the Experiment Computer that an exposure can be made by setting the signal Expose Image Area/Transmission Complete. At the end of the exposure, the Experiment Computer sets the Begin Picture Sequence/Transmit Picture signal to zero.

The Camera Microcontroller proceeds to transfer the image area to the storage area and line by line working with the Telemetry Microcontroller transmits the picture. Now that the picture has been transmitted another exposure can be made and the Expose Image Area/Transmission Complete becomes zero.

To transmit a picture the Camera Microcontroller commands the Clock Generator to:

- o Perform an Image Transfer to move the image to the storage area
- o Perform a Line Read to empty the Horizontal Register of charge
- o Perform a Line Transfer to transfer the first line into the Horizontal Register
- o Perform a Line Read operation

This puts the first pixel of line on the ADC Bus. The Telemetry Microcontroller is informed that there is data on the bus (Convert Window = 1) and loads the first pixel into the beginning of a frame. The Telemetry Microcontoller then in syncronization with telemetry, reads the rest of the picture segment of the line into telemetry via the Pixel Read command. It then returns control to the Line Read operation which reads the unused portion at the end of the line. The Camera Microcontroller repeats the Line Transfer-Line Read scenario another 255 times and the entire picture is then completely transmitted.

When the Clock Generator is in the process of executing a command, it generates a signal called Busy which informs the CCD Microcontroller of its status. The Enable ADC signal as the name implies allows the ADC to convert the pixel analog signal into digital data. It is also used to specify that the Camera is no longer in the erase routine and the output of the CCD is a valid picture signal and not thermal noise.

3.3.3 Correlated Double Sample and Hold Module

The correlated double sample and hold module samples and quantizes the analog output of the CCD preamplifier. The Clock Generator produces the timing signals for this function. These signals are called: Suppress (SUPRN), Clamp (CLAMPN), and Sample (SAMPN). The analog signal is an output from the CCD Head

Electronics package where the preamplifier is located. The Correlated Double S/H module consists of a single printed circuit in the Camera Electronics package.

To understand the operation of the Correlated Double S/H it is useful to discuss the nature of the video signal generated in the CCD image sensor and the information desired from it. The CCD signal charge is collected in the floating diffusion gate of the CCD output transistor. Before a new charge is shifted to this floating diffusion gate, the previous charge is removed by "resetting" it to a positive potential. A large voltage spike is produced due to this reset pulse. The voltage level output which follows is essentially equal to the voltage produced from a pixel containing no charge (background level). See Figure 4. The next charge transferred to the floating diffusion gate produces a proportional output voltage which is labeled "pixel charge level" in the figure. The function of the Correlated Double S/H is to generate a voltage proportional to the difference between the pixel charge level and the background level.

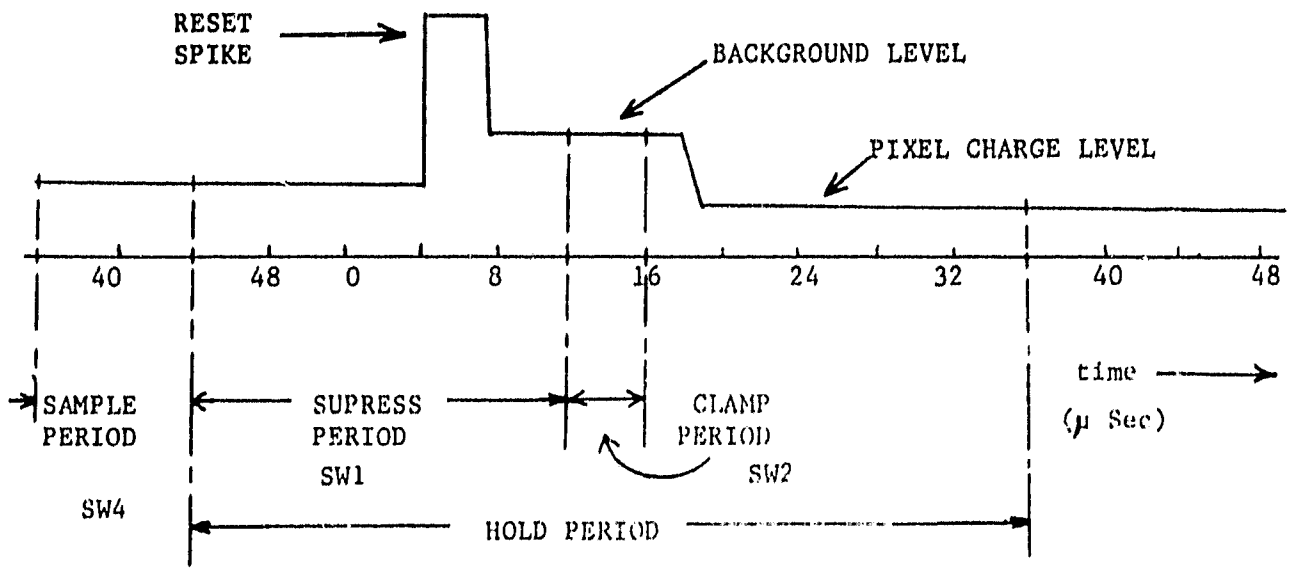


Figure 4. Sample and Hold Input Waveform

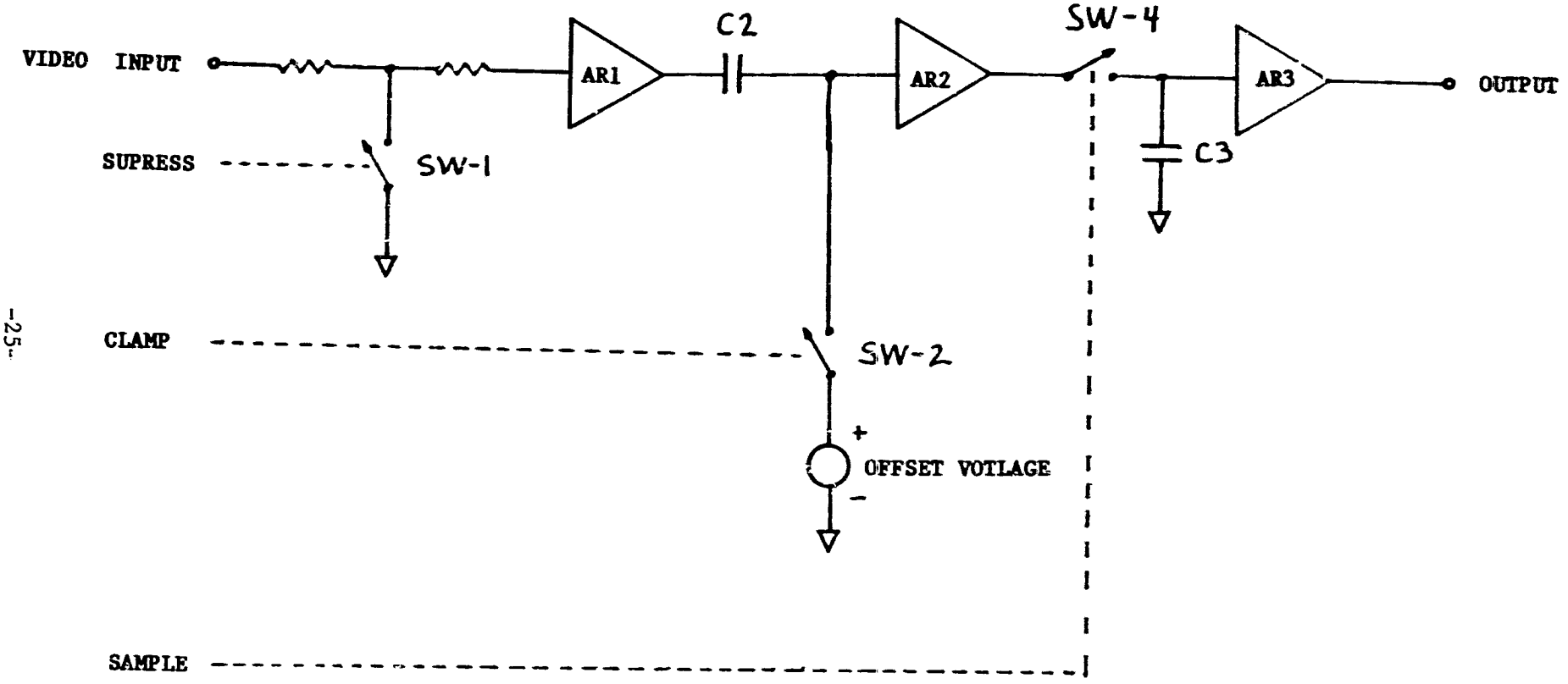


Figure 5. Correlated Double Sample and Hold Block Diagram

The time periods shown in Figure 4 are based on a 52 microsecond pixel period. A simplified block diagram of the circuit is shown in Figure 5 where the mechanical switches are symbolic for the solid state analog switches actually used.

Switch 1 closes 4 microseconds after the end of the previous "sample" period. It remains closed until the start of the "clamp" period. The purpose of this is to reduced the noise and transient effects of the reset spike. The inverted stage of AR1 has a gain of -3.5. During the "clamp" period Switch 2 is closed and C2 is charged to a voltage proportional to the difference of the analog input and the background level (plus a small offset). Switch 4 closes 20 microseconds later, "turning on" AR2 and connecting C3 to its output. C3 then charges to the new pixel level. AR2 is "turned off" during the "hold" period by reducing the currents in its internal current sources. The voltage output of AR2 will change little during this time, thus reducing the effects of capacitive coupling across Switch 4, which is open, on the voltage of C3 during the "hold" period. AR3 is used as a buffer between C3 and the A/D converter. An offset voltage is generated to correct for offsets introduced in the analog circuits and is used to define an output of -5.0 volts as "black",i.e., no pixel charge.

3.3.4 The ADC Module

The ADC Module is a single printed circuit board which transforms the quantized output of the Correlated Double Sample and Hold circuit into an 8-bit digital word. It has two control inputs: the Convert (CONV) and the Enable ADC (ENADC) signals. The Convert signal comes from the Clock Generator. It starts the analog to digital conversion when the output of the sample and hold is stable. The Enable ADC signal allows conversions to occur and inhibits conversion of pixels which are read in the erase routine. For the Data Output Mode of camera operation the ADC Module generates a signal called Data Present which equals one when data is valid on the Data Output Bus. Data Present is used to load the data into the external imaging system.

The key device in this module is the Micro Networks MN5240 high speed successive approximation analog to digital converter. The converter is used in the

bipolar input configuration resulting in a +5 to -5 volt input range. The output coding of the module in base 16 (hexidecimal) is 00 for -5.0 volts input, 80 for 0 volts input, and FF for +4.9609 volts input. The conversion time is less than 4 microseconds.

3.3.5 Telemetry Interface Module

The Telemetry Interface Module controls the Clock Generator and interfaces the CCD Camera to telemetry. It is responsible for synchronizing the reading of a picture to the telemetry data rate.

The module consists of a single printed circuit board. The three control signals to and from the Clock Generator Module are: Enable ADC (ENADC), Pixel Read (PR), Convert Window (CONV WIND). The two data buses that send information to the module are the ADC Data Bus (from the ADC Module) and the Experiment Data Bus (from the Experiment Computer). The output bus to telemetry is the Telemetry Data Bus. Main Frame Synchronization (MFS) and Word Synchronization (WS) are signals from telemetry used for real time data synchronization. All data buses are eight bits wide.

The key device in the module is an Intel 8748 single chip 8-bit microcomputer with 1K of erasable and programmable program memory and 64K bytes of RAM, the same device used in the Camera Microcontroller Module. The EPROM program stores information on where data is to be located in the telemetry frame and how it is to be transferred. A new frame format can be created easily and simply by changing the program in the microcontroller.

3.3.6 Telemetry Formatting

The standard sounding rocket telemetry system, developed by the Physical Science Laboratory of the University of New Mexico for solar payloads, has a frame consisting of 32 words each 12 bits wide and a frame rate of 1024 frames per second. The first two words contain information used for coding the telemetry transmission. This leaves 30 words per frame for experiment data. In the present configuration eight of these words contain pixel intensity data, two words pixel location data, one word the exposure and filter type, and one word

the type of frame being transmitted. All of these data are represented by 8-bit words. This format was chosen to minimize changes to the existing software used to display the images in real time.

The CCD Camera formats three frame types during the flight. The frame types are called Empty Frame, Picture/No Pixels, and Picture/Pixels. These three frame types are a requirement of the real-time imaging system software of the ground support equipment. The Empty Frame is the telemetry frame transmitted during periods when the camera is not reading the CCD, when it is in an idle period or when it is exposing the CCD. Besides the frame type data word which specifies an Empty Frame, it contains the exposure/filter data word from the Experiment Computer. The Picture/No Pixels is a frame transmitted during the reading of pixels which are not converted into data. In addition to frame type and exposure/filter words it contains the two words which specify the location in the CCD array of the pixel data in the frame. This location is specified in X and Y coordinates. The pixel address (X,Y) in a Picture/No Pixel frame type is the address of the first pixel in the next line. Thus, if the current line is N, then as the end of N is read the Picture/No Pixels address is (0, N+1).

The third frame type, Picture/Pixels, is transmitted during the reading of an active section of a line in the CCD array. It is in this frame type that the image data is transmitted. The data words in this frame are: the eight pixel intensity words, the X address, the Y address, the exposure/filter, and the frame type. The (X,Y) address is the address of the current pixel group of the particular frame.

3.3.7 Frame Synchronization and Subroutine Selection

The telemetry microcontroller is synchronized to telemetry by the Main Frame Sync (MFS) and Word Sync (WS) signals. At the beginning of a frame MFS is one. MFS is used by the microcontroller as an interrupt signal which causes the program to jump to program memory location 3. When this occurs the program goes to a routine whose address is selected by the signals from the Clock Generator Module. The Enable ADC and Convert Window signals specify the status of the camera and also identify the program memory address of the routine named for the frame type to be transmitted. If both signals are zero then the camera is

in an idle period and the address is the Empty Frame Routine. This routine formats the frame with words 28 and 31 (see Table 1, Frame Format).

When the Camera begins the reading of the image stored in the CCD storage area the Enable ADC signal becomes one and the Convert Window signal remains zero. The program memory address mapped by ENADC=1 and CONV WIND=0 is the address of the Picture/No Pixels Routine. The Picture/No Pixels Routine formats the frame with words 2,3,28 and 33. As described earlier (Section 3.3.1) not all the pixels in a line are converted into intensity data for transmission. These pixels may be at the beginning of a line, at the end of a line, or both at the beginning and end of a line depending on the raster limit settings. For this reason there are no pixel intensity words in this frame type which occurs between the Picture/Pixels frames. The pixel address, words 2 and 3, is of the next pixel group to be read. This information is needed by the real-time imaging software. Since there is only one X-address per frame, only the location of the first pixel in the frame is specified since this locates the entire group.

The Convert Window signal is one only during the reading of those pixels in a line which are to be reconstructed into an image. This is true for 256 of the 320 pixels in a line. The program memory address mapped by ENADC=1 and CONV WIND=1 is therefore the address of the Picture/Pixels Routine. This routine formats the frame with the additional pixel intensity words and it runs during the transmission of the image data. All the experiment information is present in this frame.

3.3.8 Word Synchronization

The telemetry frame is formatted in real time by shifting data from a holding register to the telemetry data bus word by word. This register serves as a temporary storage register for the experiment data. The shift occurs on the leading edge of the Word Sync signal and places the contents of holding register on the bus for one word period (30.52 microseconds). Data is loaded into the holding register under the control of the microcontroller. To the micro-

Table 1

FRAME FORMAT

	MSB											LSB	
Bit #	1	2	3	4	5	6	7	8	9	10	11	12	
Word #													
0					Frame Synchronization								First Word
1					Words								Transmitted
2	0	0	0	0	Z1	Z1	Z1	Z1	Z1	Z1	Z1	Z1	
3	0	0	0	0	X	X	X	X	X	X	X	X	
4	0	0	0	0	Y	Y	Y	Y	Y	Y	Y	Y	
5					-0-								
6	0	0	0	0	Z2	Z2	Z2	Z2	Z2	Z2	Z2	Z2	
7					-0-								
8					-0-								
9					-0-								
10	0	0	0	0	Z3	Z3	Z3	Z3	Z3	Z3	Z3	Z3	
11					-0-								
12					-0-								
13					-0-								
14	0	0	0	0	Z4	Z4	Z4	Z4	Z4	Z4	Z4	Z4	
15					-0-								
16					-0-								
17					-0-								
18	0	0	0	0	Z5	Z5	Z5	Z5	Z5	Z5	Z5	Z5	
19					-0-								
20					-0-								
21					-0-								
22	0	0	0	0	Z6	Z6	Z6	Z6	Z6	Z6	Z6	Z6	
23					-0-								
24					-0-								
25					-0-								
26	0	0	0	0	Z7	Z7	Z7	Z7	Z7	Z7	Z7	Z7	
27					-0-								
28	0	0	0	0	E	E	E	E	E	E	F	F	
29					-0-								
30	0	0	0	0	Z8	Z8	Z8	Z8	Z8	Z8	Z8	Z8	Last Word
31	0	0	0	0	T	T	T	T	T	T	T	T	Transmitted

Character:	Description:
E	Exposure Period
F	Filter Number
T	Frame Type
X	X Pixel Address
Y	Y Pixel Address
Z	Pixel Intensity
-0-	Word Data All Zeros

controller this register is seen as external memory and all write instructions are to this device. The controller reads data from three sources: the ADC Data Bus, The Experiment Data Bus, or an internal register. During any word period the controller must load the holding register with the data for the next word. To accomplish this, the controller needs to know where it is in the frame at all times. As explained above the beginning of the frame occurs when MFS becomes one. This signal, used as an interrupt signal, synchronizes the program to the beginning of the frame. The first two words of the frame are provided by telemetry giving the controller 63.0 microseconds to select the proper frame routine and load the latch with the third word of the frame.

Word synchronization is accomplished by testing the Word Sync signal. If the Word Sync becomes one, the controller knows the data stream is at the beginning of a word. It then can load the holding register with the next data to be transmitted. The type of data loaded is dependent on the program. During a word period the controller can either read the ADC Data Bus and store it in the holding register; read the Experiment Data Bus and store it in the holding register; or store the contents of an internal register in the holding register. This allows the selection of the type of data for each word in a frame to be under program control.

3.3.9 CCD Readout and Synchronization

Upon receiving a Transmit Picture signal from the Experiment Computer, the CCD Microcontroller transfers the picture from the Image Area to the Storage Area and transfers the first line of the picture to the Horizontal Register. Next the CCD Microcontroller reads the line up to and including the first pixel to be transmitted and passes control of the Clock Generator to the Telemetry Microcontroller. The first pixel intensity data now resides on the ADC Data Bus and the clocking of the horizontal register stops.

Before the CCD Microcontroller received the transmit picture command the frame type status was of the Empty Frame type. When the transmit picture command is received the frame type changes to the Picture/No Pixels frame type which specifies that the camera is transmitting a picture but there is no pixel data yet available. The Telemetry controller is processing a Picture/No Pixel frame

when it receives control of the Clock Generator. The controller is thereby instructed to transmit a line of picture information. After completion of the current picture/no pixel frame, the telemetry controller changes to the Picture/Pixels frame routine. For the next frame, the first Picture/Pixel frame, the data which is on the ADC Bus is loaded into the latch and then shifted out to the Telemetry Bus as the first pixel in the line. The controller sends a Pixel Read command to the Clock Generator which increments the Horizontal Register by one pixel and places the second pixel intensity data on the ADC Bus. Since pixels are formatted every fourth word there is sufficient time to read and store the next pixel before it is needed in the frame. In this manner the frame is loaded with eight pixel intensity words along with the other frame data. Thirty-two such frames are consecutively transmitted. The Clock Generator via the Convert Window signal informs the Telemetry Microcontroller that all the valid data in the line has been transmitted and to return to the Picture/No Pixel routine.

At this point in time the control of the Clock Generator is passed back to the CCD Microcontroller and the Clock Generator completes the reading of the current line. The CCD controller transfers the next line from the storage area to the Horizontal Register and again reads the line via the Clock Generator until it encounters the first pixel to be transmitted. Control is passed to the Telemetry controller and the line is transmitted. This process repeats until 256 lines have been transmitted. For the end of the last line the CCD Microcontroller reads the end of the line during which the telemetry frame type is the Picture/No Pixels frame type. After the last line is read the Telemetry Microcontroller returns to the Empty Frame routine specifying the end of the picture. The CCD Microcontroller signals the Experiment Computer that the picture has been transmitted and it returns to the Erase Routine. This routine cleans the image area of charge which has accumulated during the picture transmission.

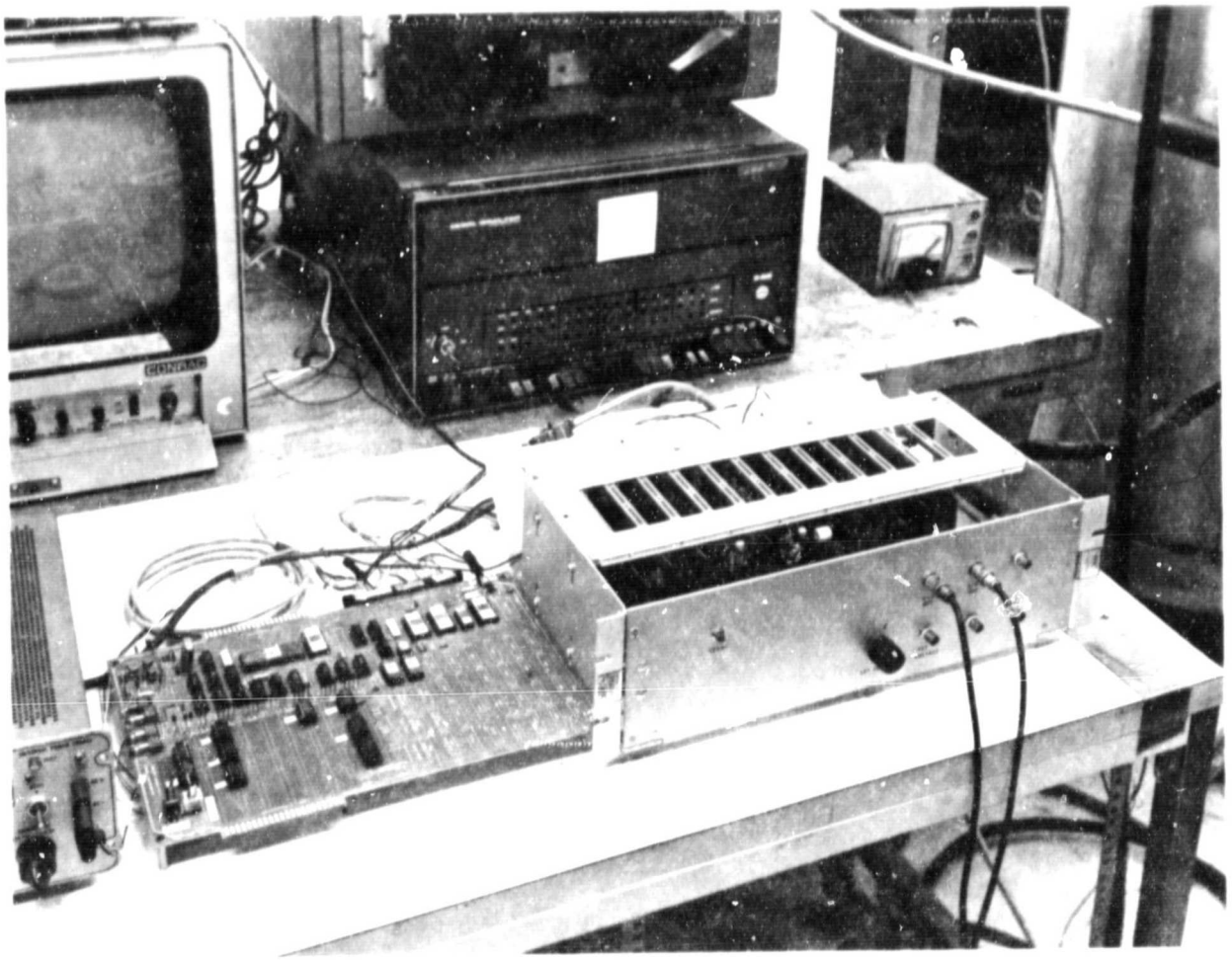
4.0 RESULTS AND CONCLUSIONS

Preliminary testing of the camera has been performed in our laboratory and is continuing under follow-on contract NASW-3924. The CCD Test Set is shown in Figures 6, 7 and 8. Figure 6 shows the control and display electronics. In the foreground is the camera breadboard (right) and the experiment computer (left). The camera breadboard was designed as a series of cards each of which performs a specific function or functions. The layout of the flight camera follows the same format which allows the flight cards to be troubleshooted and tested individually in the breadboard camera before incorporation into the flight camera.

The Experiment Computer controls the camera shutter and at the end of each exposure transmits the image data to the Image Display Computer (right background) for display on the video monitor. The Experiment Computer allows exposure times to be set from the keyboard. During the development process this computer was also used to substitute for the camera microcontroller and was programmed to control the sequence of camera operations. Figures 7 and 8 show the vacuum system and supporting equipment. The system is oil free and contains all stainless steel components. Roughing is performed with sorption pumps while the high vacuum is achieved and maintained using a CTI Cryogenics cryopump. Operating pressures of 1×10^{-7} torr are readily obtained.

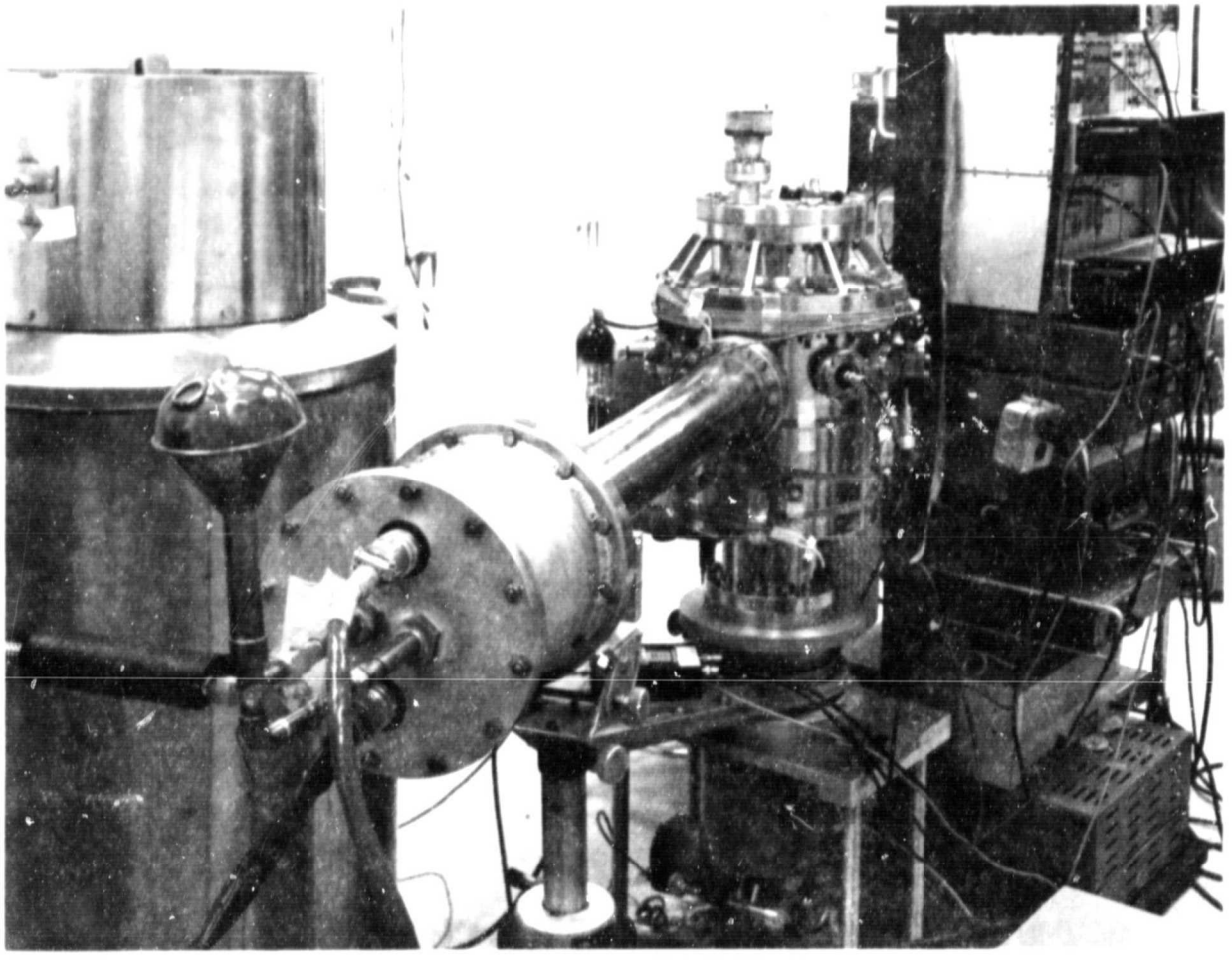
The CCD is mounted in the chamber at the left in Figure 7. Cooling is achieved with a cold finger which is attached at one end to the CCD carrier and has its other end immersed in a liquid nitrogen bath. The temperature is measured by a copper constantan thermocouple. Temperature control is achieved through the use of heaters which are attached to the CCD carrier and are activated once the desired temperature is reached. Temperatures below -120°C can be achieved with this system.

The CCD can be illuminated by either visible light or X-rays. Visible light images are obtained either by projecting an image through a port in the vacuum chamber (shown to the right of center in Figure 6) or by placing a grid directly in front of the CCD and illuminating the grid with collimated light to form a shadowgraph. X-ray images are formed by the latter technique using an X-ray



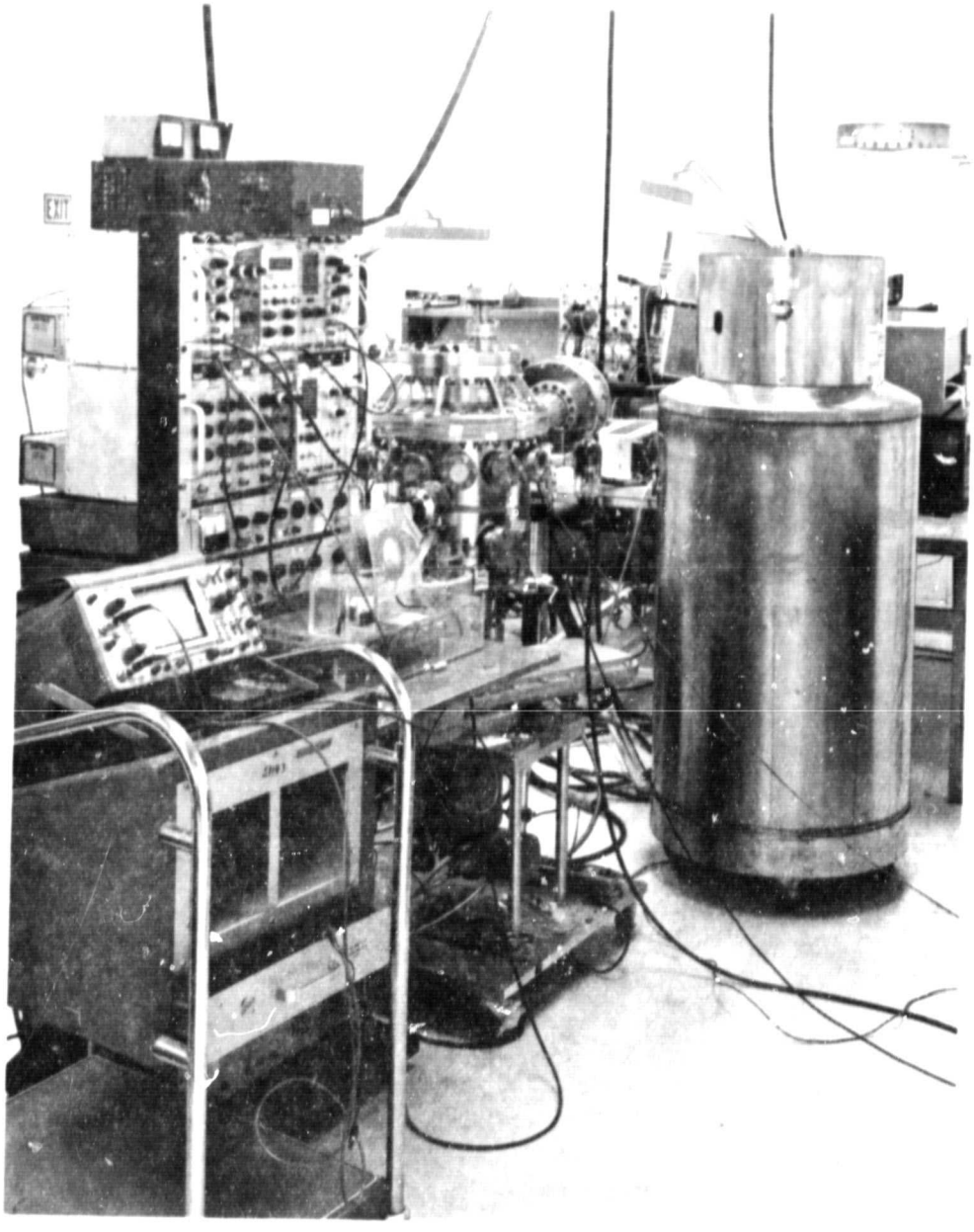
EM-472

Figure 6. Foreground: Right, CCD Camera Camera Breadboard. Left, Experiment Computer Simulator. Background: Center, Image Display Computer. Left, Video Display Monitor.



EM-471

Figure 7. CCD Test Vacuum Chamber. Foreground: CCD Camera Head Electronics Housing with Electrical and Liquid Nitrogen Feedthrough, Optical Bench. Background: X-Ray Source Chamber and Cryopump.

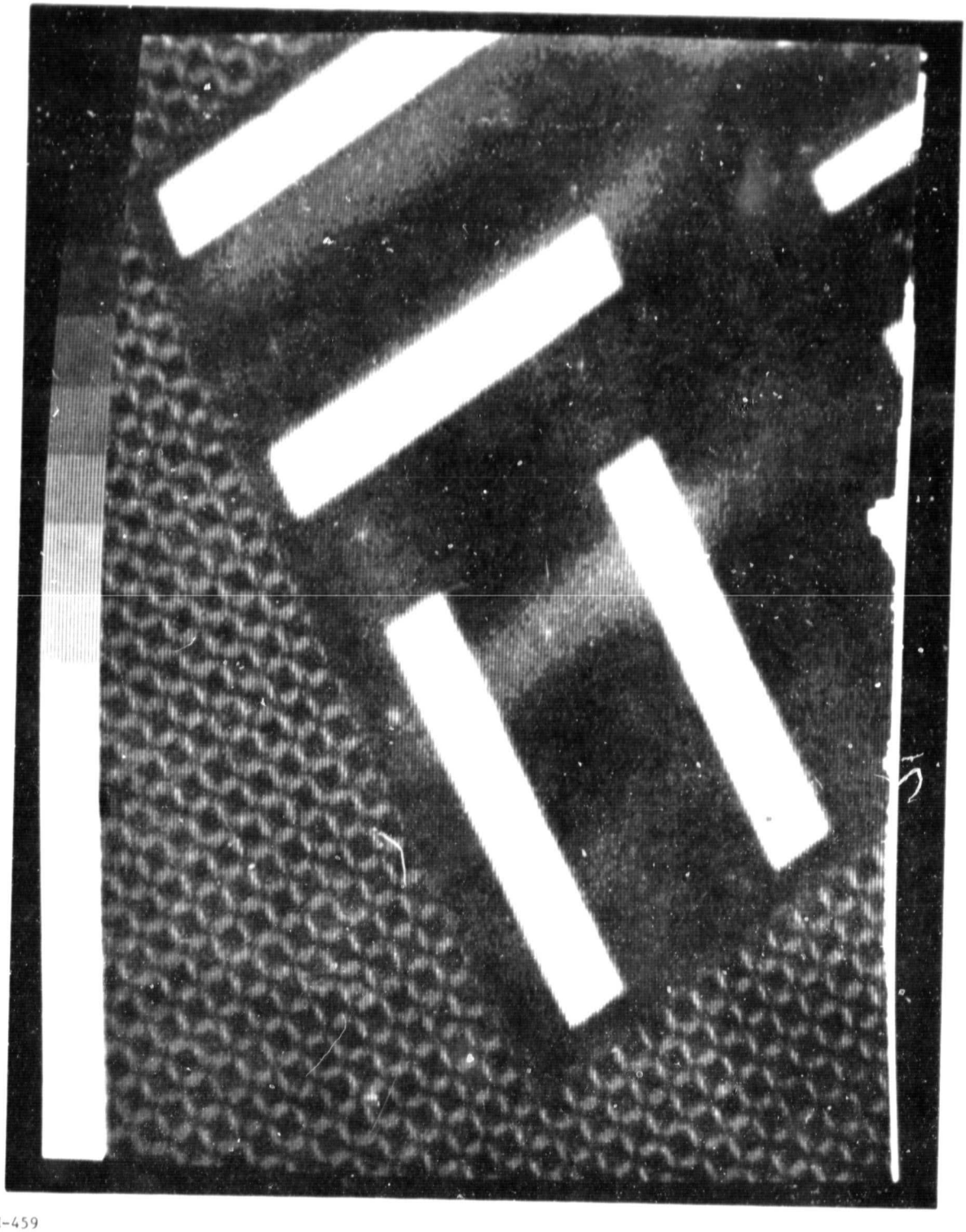


EM-473

Figure 8. X-Ray Production and Monitoring Equipment. Foreground: Monitor Oscilloscope. Rack: Filament and Anode Power Supplies, X-Ray Photon Counting Equipment.

source located in the rear chamber at a distance of approximately 122 cm from the CCD. The X-rays are generated by electron bombardment of various anode materials held at a potential, or in practice a factor of 2 above, equivalent to the energy of the X-ray line to be generated. The electron source is a hot filament and care has to be taken to shield the CCD from direct visible light by filtering. To date we have made exposures at 8.3 A (Aluminum K-alpha) and 43.6 A (Carbon K-alpha). An image of a grid consisting of a fine mesh and larger bars photographed from the monitor screen is shown in Figure 9. The CCD was illuminated with carbon X-rays using an exposure time of 6 minutes. It confirms that the CCD is sensitive to these wavelengths. The absolute sensitivity of the CCD can be evaluated by comparison with a proportional counter mounted in the same plane as the CCD.

Current testing has demonstrated the functional performance of the camera. The actual calibration and measurements of absolute sensitivity as a function of wavelength, charge transfer efficiency as a function of temperature, etc., will be performed under Contract NASW-3942 and will be described in the final report of that contract.



EM-459

Figure 9. A Shadowgraph taken at 44 A with the CCD Camera. The Exposure Time was 6 Minutes.

APPENDIX A: Signal Symbol Definitions

Name	Function
CLK	Clock-CCD Camera clock bus
CSN	The chip enable signal from the Clock Control Board. It puts the EPROM in the Active mode when equal to zero.
A0-A7	These are the eight address lines for the EPROM on the the Memory Board.
ENHN	The enable signal for the horizontal clocks and the S/H - ADC clocking.
ENAN	Enables the Image Area clocks. Signal active low.
ENA	Same function as ENAN but active high
ENBN	Enables the Storage Area clocks.
ENB	Same function as ENBN but active high
Q0	An output of the EPROM, from the memory board, this signal is used to generate the EPIXN signal which specifies the end of a timing sequence.
CLAMPN	An output of the Memory Board, this signal is used by the Correlated Sample and Hold circuit to create a black reference level
SAMPN	An output of the Memory Board, this signal is used by the Correlated Sample and Hold circuit to sample the intensity segment of the pixel video signal.
SUPRN	An output of the Memory Board, this signal is used by the Correlated Sample and Hold circuit to clamp its input to zero during the resetting of the CCD output transistor.
CONVN	An output of the Memory Board, this signal is used by the ADC Board to begin the conversion
VH1, VH2, VH3	These three signals are outputs of the Memory Board and are used by the CCD Camera Head electronics to shift the horizontal register.
VR	An output of the Memory Board, this signal is used by the CCD Camera Head electronics to reset the CCD output transistor.

VA1, VA2, VA3	These three signals are outputs of the Memory Board and are used by the CCD Camera Head electronics to shift the image or A register.
VB1, VB2, VB3	These three signals are outputs of the Memory Board and are used by the CCD Camera Head electronics to shift the storage or B register
LT	Line Transfer - Input to the Clock Control Board performs line transfer operation
IT	Image Transfer - Input to the Clock Control Board performs image transfer operation
LR	Line Read - Input to the Clock Control Board performs line read operation
PR	Pixel Read - Input to the Clock Control Board performs the reading of a pixel
BUSY	Output of the Clock Control Board is high when the CCD clocks are active
ENADC	Output of the CCD Microcontroller which enables the ADC and specifies the reading of a picture
CONV WIND	Convert Window-Output of the Raster Limit Board which equals one to convert into data a section of the horizontal register
ANLG INPUT	Analog Input-The video input to the sample and hold circuit from the Camera Head Electronics package
ANLG SHLD	Analog Shield-the shield of the coaxial cable that sends the video signal to the sample and hold circuit
AN +15	Analog +15 volt supply bus
AN -15	Analog -15 volt supply bus
AN GND	Analog ground bus
DIG +5	Digital +5 Volt supply bus
DIG GND	Digital ground bus
VIDEO OUT	Video Output-The video output from the S/H board to the ADC board
VIDEO RTN	Video Return-Ground connection for the shield of the VIDEO OUT signal form the S/H board

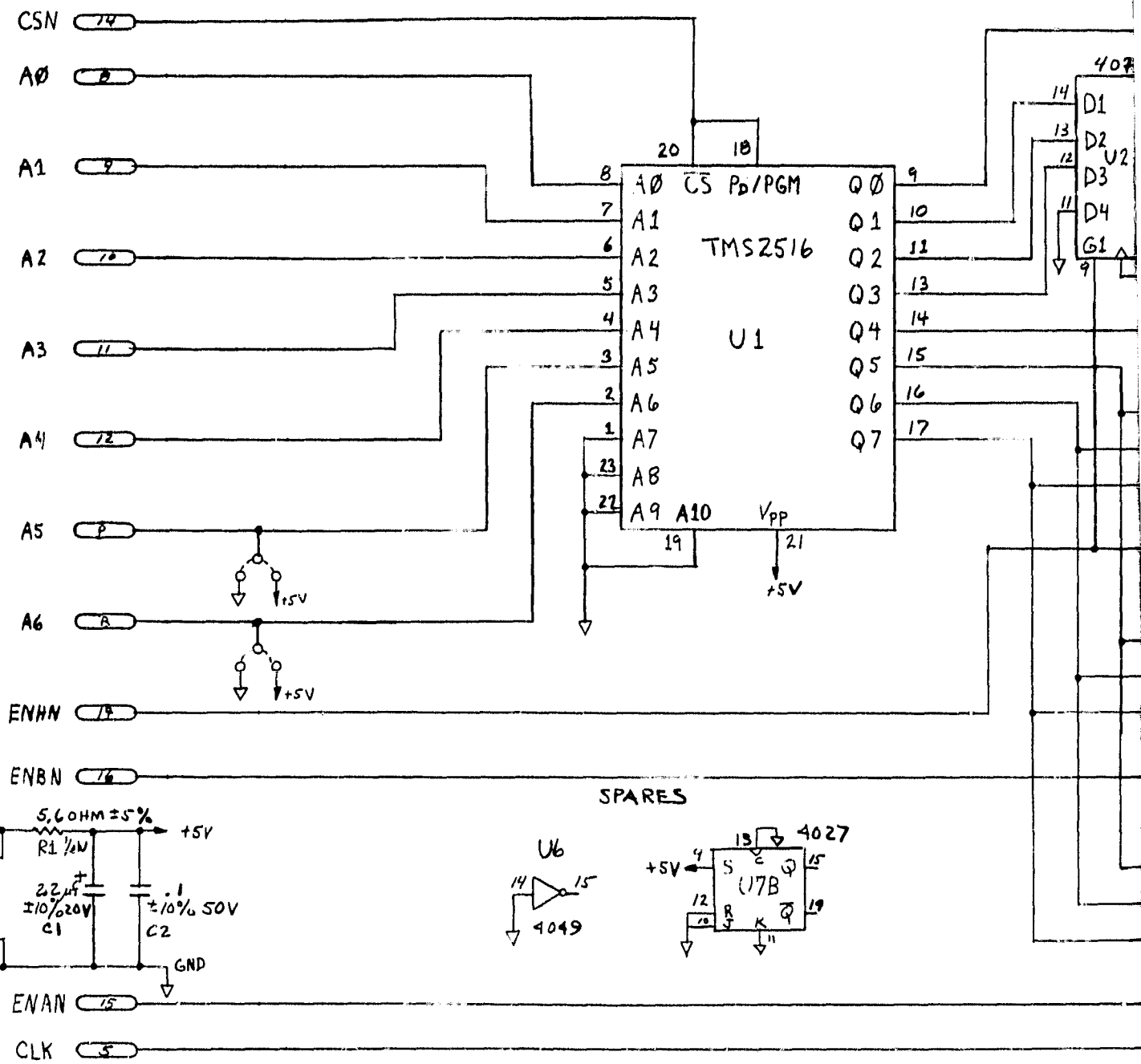
REML	Reset Multiple Line-Signal from the Raster Limit board to the Clock Control board specifies the end of a line or the end of an image transfer operation
RESL	Reset Single Line-Signal on the Clock Control board specifies the end of a pixel clocking sequence
DATA/TLM	Data/Telemetry Output Select input to the Clock Control board. Equals one to put the camera in the Data Output Mode Equals zero for the Telemetry Output Mode
EPIXN	End of Pixel-Output of the Clock Control board Active low specifies the end of a pixel clocking sequence.
RECON	Output of the Clock Control board and enable signal for logic circuits active low
MASTER CLOCK INPUT	External clock signal fed to the Clock Control board it is divided down to the clock bus frequency
BPS/TPN	Begin Picture Sequence/Transmit Picture is a signal from the Experiment Computer to the Camera Microcontroller. A zero to one transition signals the camera system to begin a picture sequence. A one to zero transition signals the camera system to transmit a picture.
EIA/TCN	Expose Image Area/Transmission Complete is a signal from the Camera Microcontroller to the Experiment Computer. A zero to one transition signals the Experiment Computer to expose the CCD to the image via the shutters. A one to zero transition signals the Experiment Computer that the camera has completed the current picture.
D0-D7	These are the eight signals from the Telemetry Microcontroller to the Telemetry system. This bus contains the experiment data which is primarily picture data.
ADC0-ADC7	These are the eight signals from the ADC Board. This bus contains Pixel Intensity data.
EXP0-EXP7	These are the eight signals from the Experiment Computer. This bus contains data from this computer.

APPENDIX B: CCD Camera Drawing List

SCHEMATICS:

Name	Drawing Number
Memory Board, Board B - 27.074 CCD Camera	652-4100
Raster Limit Board, Board D - 27.074 CCD Camera	652-4101
Camera Microcontroller Board, Board J - 27.074 CCD Camera	652-4102
ADC Board, Board I - 27.074 CCD Camera	652-4103
Correlated Double Sample/Hold Board, Board H - 27.074 CCD Camera	652-4104
Clock Control Board, Board A - 27.074 CCD Camera	652-4105
Telemetry Microcontroller Board, Board K - 27.074 CCD Camera	652-4106
CCD Head Electronics Board - 27.074 CCD Camera	652-4107

APPENDIX C: CCD Camera Electronic Schematics



IC		+5V	GND	REF DES
MC14050B		1	8	U8, U9
TMS2516		24	12	U1
MC14076B		16	8,15,10	U3, U4, U5
MC14049UB		1	8	U6
MC14027B		16	8	U7
MC14076B		16	8,15,10	U2

QTY REQ'D	FIND NO.	DWG SIZE	PART OR IDENTIFYING NO.

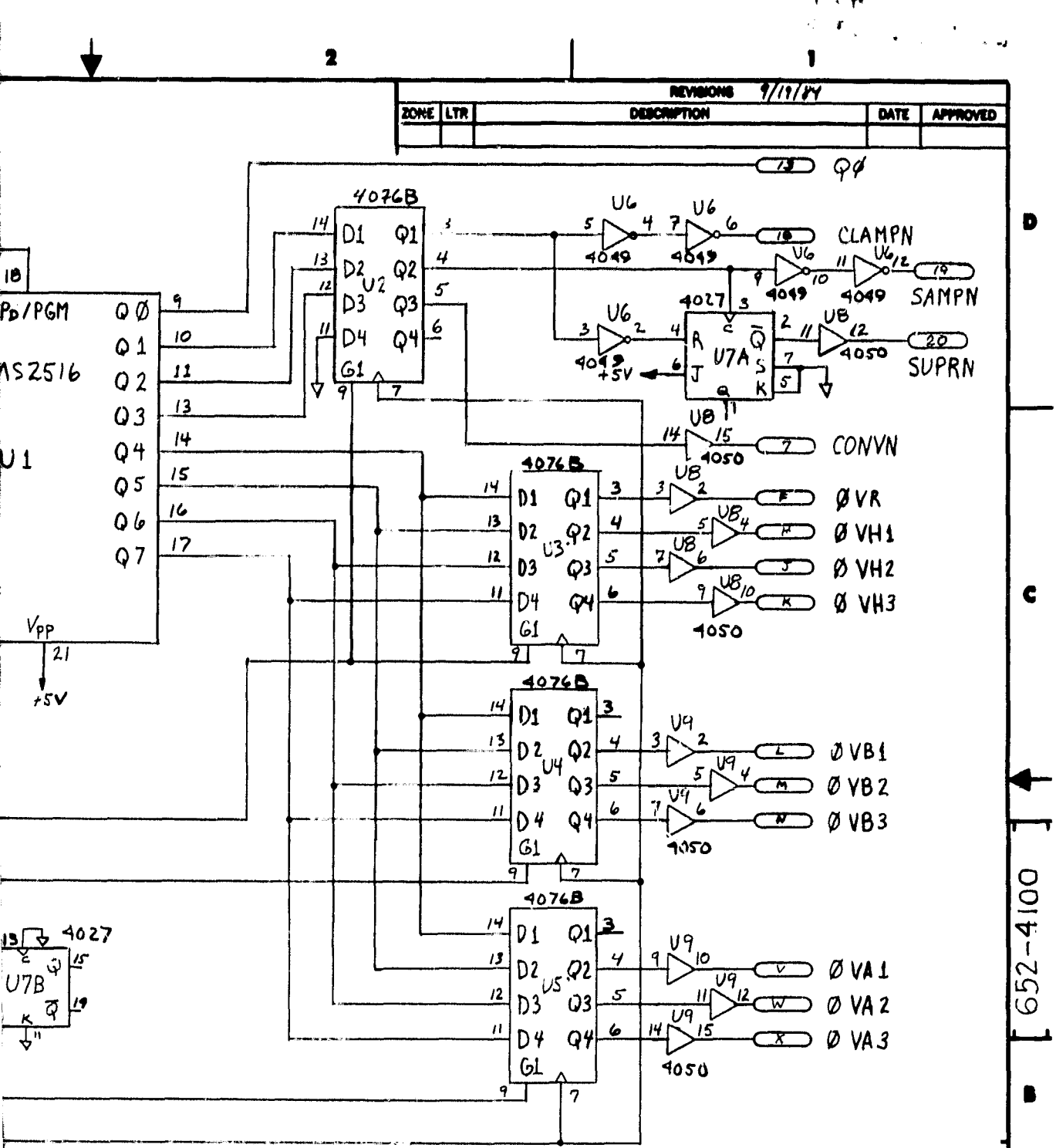
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES.
TOLERANCE ON
DECIMALS FRAC ANGLES
XX ± — ± — ± —
XXX ± —
CONCENTRICITY .005 TIR
REMOVE BURRS & SHARP EDGES
ALL MACHINED SURFACES 125 ✓
DO NOT SCALE THIS DRAWING
MATERIAL
FINISH

CONTRACT
DRAWN
CHECK
MFG
ENGR MECH
PROJECT ENGR
ADDNL APPD

NEXT ASSY USED ON
APPLICATION

BRUNING 44 232 30433 9

FOLDOUT FRAME



QTY REQ'D	FIND NO.	DWG SIZE	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	NOTE

PARTS LIST

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES.
TOLERANCE ON
DECIMALS FRAC ANGLES
.XX ± — ± — ± —
.XXX ± —
CONCENTRICITY .005 TIR
REMOVE BURRS & SHARP EDGES
ALL MACHINED SURFACES 125 ✓
DO NOT SCALE THIS DRAWING
MATERIAL
FINISH

CONTRACT NO.

DRAWN	Ray Countryman	12/19/83
CHECK		
MFG		
ENGR MECH	ENGR ELEC	Ray Countryman
PROJECT ENGR	QUAL ASSUR	
ADDNL APPD		

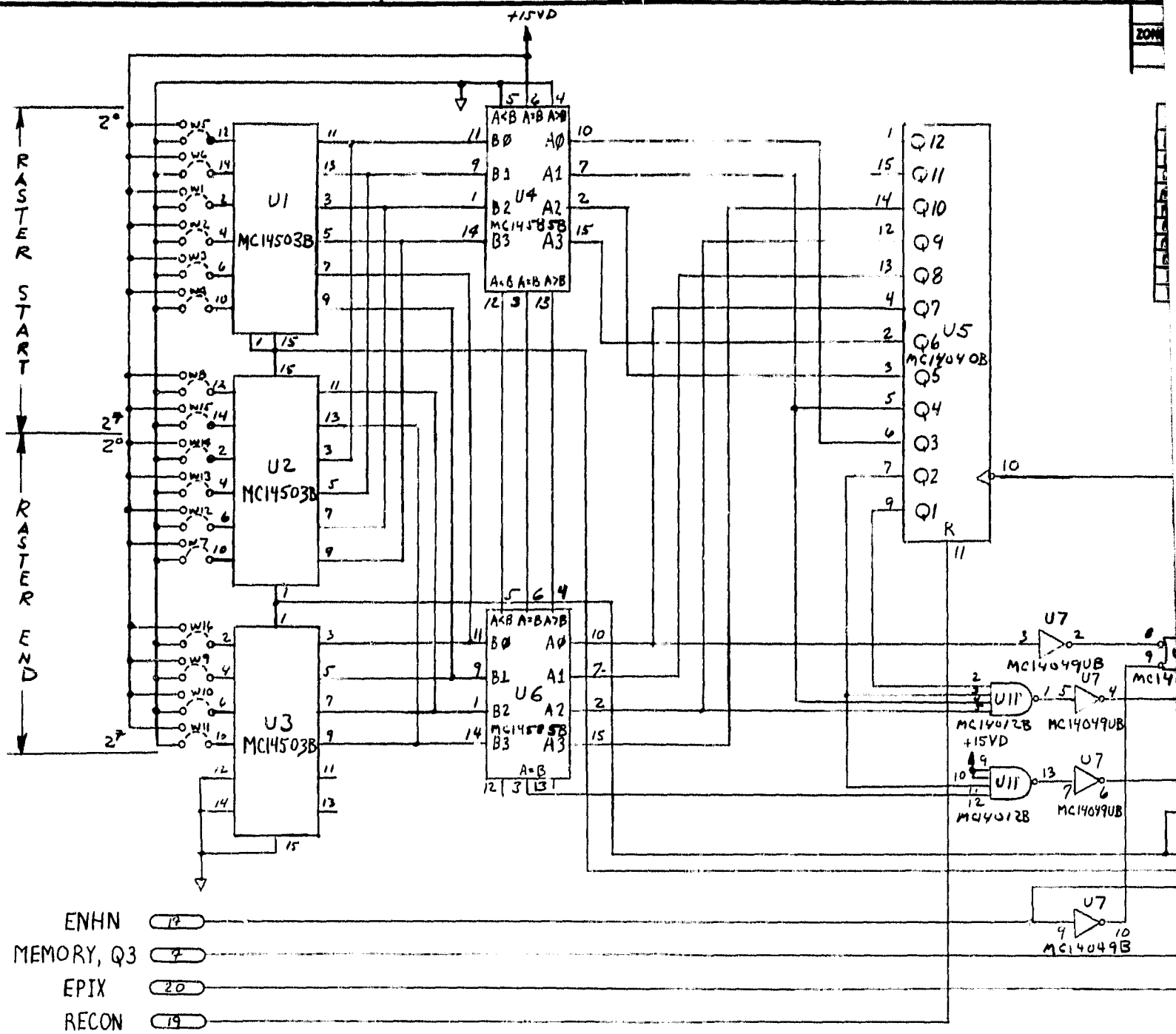
AMERICAN SCIENCE AND ENGINEERING
CAMBRIDGE, MASS.

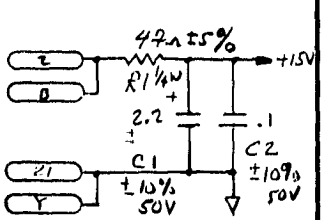
SCHEMATIC
MEMORY BOARD B
27.074 CCD CAMERA

SIZE	CODE IDENT NO.		REV
C	21802	652-4100	—
SCALE NONE			SHEET 1 OF 1

2 1

FOLDOUT FRAME





QTY REQ'D	FIND NO.	DWG SIZE	PART OR IDENTIFYING NO.

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INTERPRET THIS DRAWING IN ACCORDANCE WITH DOD-STD-100.

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES.
TOLERANCE ON
DECIMALS FRAC ANGLES
XX ± — ± — ± —
XXX ± —
CONCENTRICITY .005 TIR
REMOVE BURRS & SHARP EDGES
ALL MACHINED SURFACES 125 ✓
DO NOT SCALE THIS DRAWING
MATERIAL
FINISH

CONTRACT NO.

DRAWN	Ray Count
CHECK	
MFG	
ENGR MECH	
PROJECT ENGR	
ADDNL APPD	

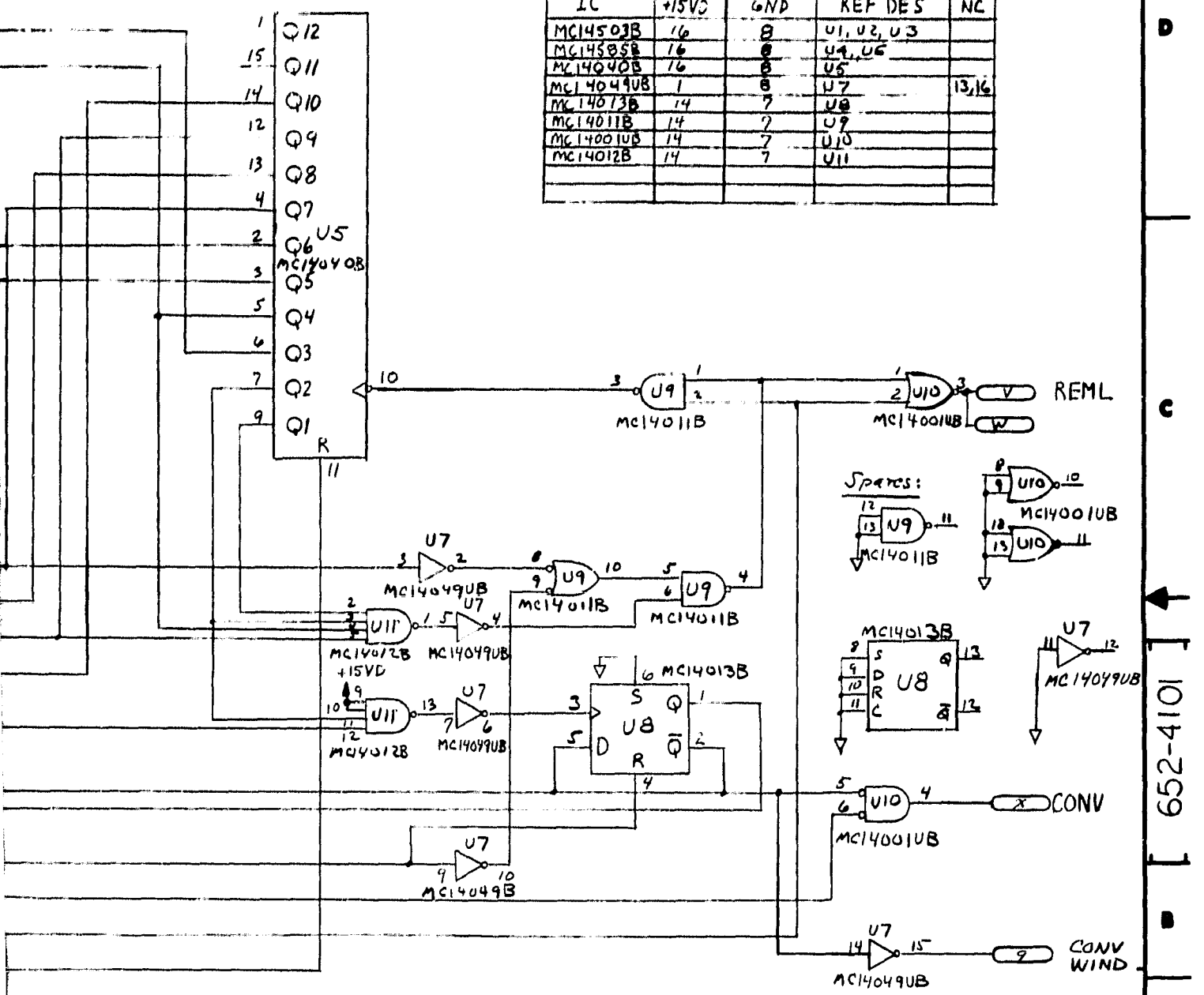
NEXT ASSY | USED ON
APPLICATION

BRUNING 44-232304339

FOLDOUT FRAME

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

IC	+15VD	GND	REF DES	NC
MC14503B	16	8	U1, U2, U3	
MC14585B	16	8	U4, U6	
MC14040B	16	8	U5	
MC14049UB	1	8	U7	13,16
MC14013B	14	7	U8	
MC14011B	14	7	U9	
MC14001UB	14	7	U10	
MC14012B	14	7	U11	



652-4101

QTY REQ'D	FIND NO.	DWG SIZE	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	NOTE
				PARTS LIST		

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES.
TOLERANCE ON
DECIMALS FRAC ANGLES
XX ± — ± — ± —
XXX ± —
CONCENTRICITY .005 TIR
REMOVE BURRS & SHARP EDGES
ALL MACHINED SURFACES 125 ✓
DO NOT SCALE THIS DRAWING
MATERIAL
FINISH

CONTRACT NO.

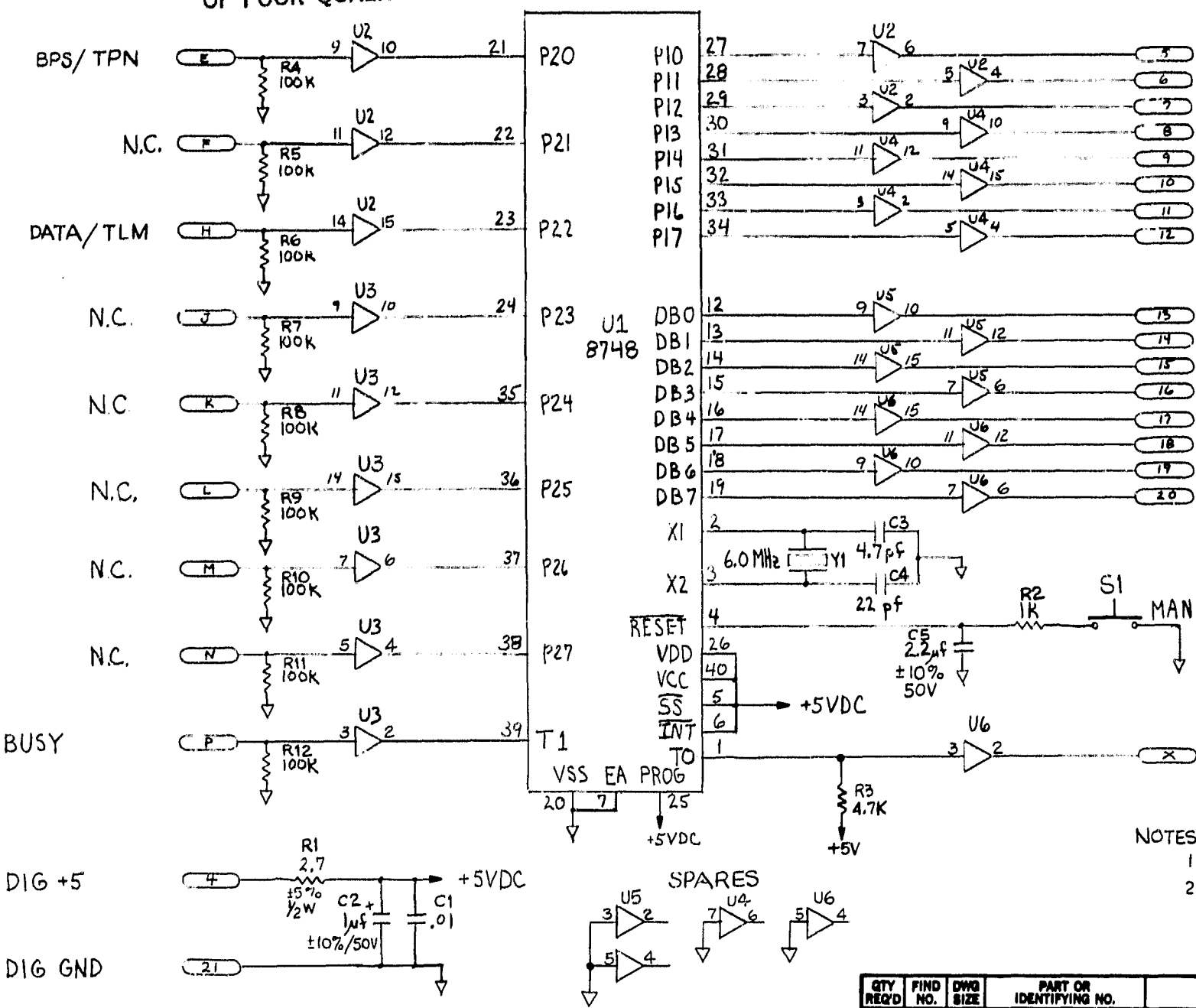
DRAWN	Ray Countermen	12/20/83
CHECK		
MFG		
ENGR MECH	ENGR ELEC	R Countermen
PROJECT ENGR	QUAL ASSUR	
ADDNL APPD		

AMERICAN SCIENCE AND ENGINEERING
CAMBRIDGE, MASS.

27.074 CCD CAMERA TEST SET
RASTER LIMIT BOARD D
SCHEMATIC

SIZE	CODE IDENT NO.		REV
C	21802	652-4101	—
SCALE			SHEET 1 of 1

NEXT ASSY USED ON
APPLICATION



NOTES:
1. AL
2. AL

QTY REQ'D	FIND NO.	DWG SIZE	PART OR IDENTIFYING NO.

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES.
TOLERANCE ON
DECIMALS: .XX ±, .XXX ±
FRAC ±
ANGLES ±
CONCENTRICITY .005 TIR
REMOVE BURRS & SHARP EDGES
ALL MACHINED SURFACES 125 ✓
DO NOT SCALE THIS DRAWING
MATERIAL
FINISH

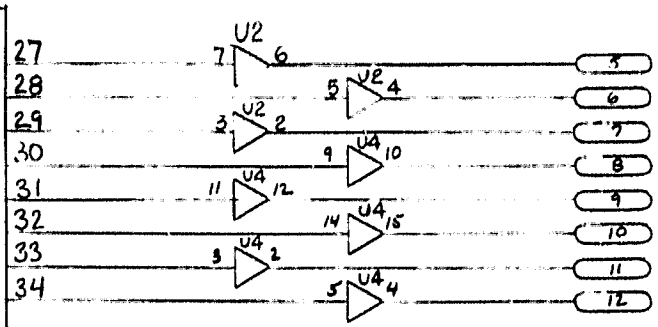
CONTRACT NO.

DRAWN	R Courte
CHECK	
MFG	
ENGR MECH	
PROJECT ENGR	
ADDNL APPD	

BRUNING 44-232-304339

FOLDOUT FRAME

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



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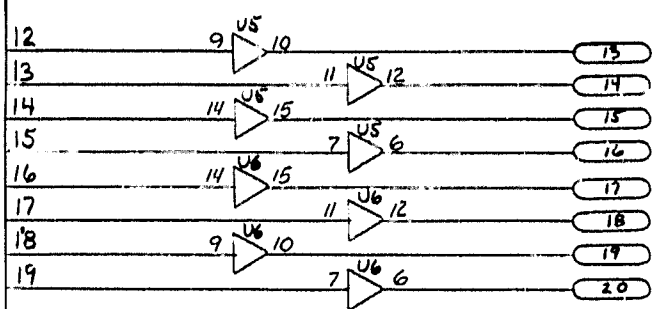
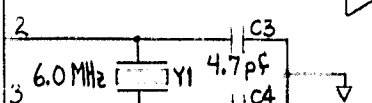
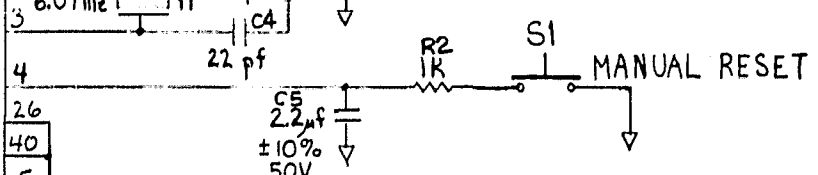
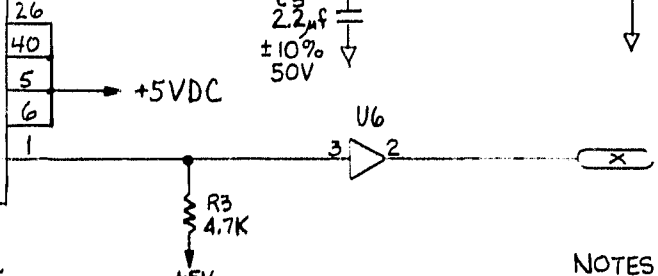


EIA/TCN
NC
NC
ENADC
NC
NC
NC
NC







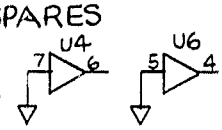
Controller Clk
2 MHz

IC	+5VDC	GND	REF DES
MC14050B	1	8	U2, U3, U4, U5
			U6

652-4102

NOTES:
1. ALL RESISTORS ARE ±5%, ¼W
2. ALL CAPS ARE ±10%, 50V UNLESS NOTED

SPARES



QTY REQ'D	FIND NO.	DWG SIZE	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	NOTE

PARTS LIST

DXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES.
TOLERANCE ON
DECIMALS FRAC ANGLES
XX ± ± ±
XXX ± ± ±
CONCENTRICITY .005 TIR
REMOVE BURRS & SHARP EDGES
ALL MACHINED SURFACES 125 ✓
DO NOT SCALE THIS DRAWING
MATERIAL
FINISH

CONTRACT NO.

DRAWN	R Counterman	7/3/84
CHECK		
MFG		
ENGR MECH	ENGR ELEC	R. Counterman
PROJECT ENGR	QUAL ASSUR	
ADDNL APPD		

AMERICAN SCIENCE AND ENGINEERING
CAMBRIDGE, MASS.

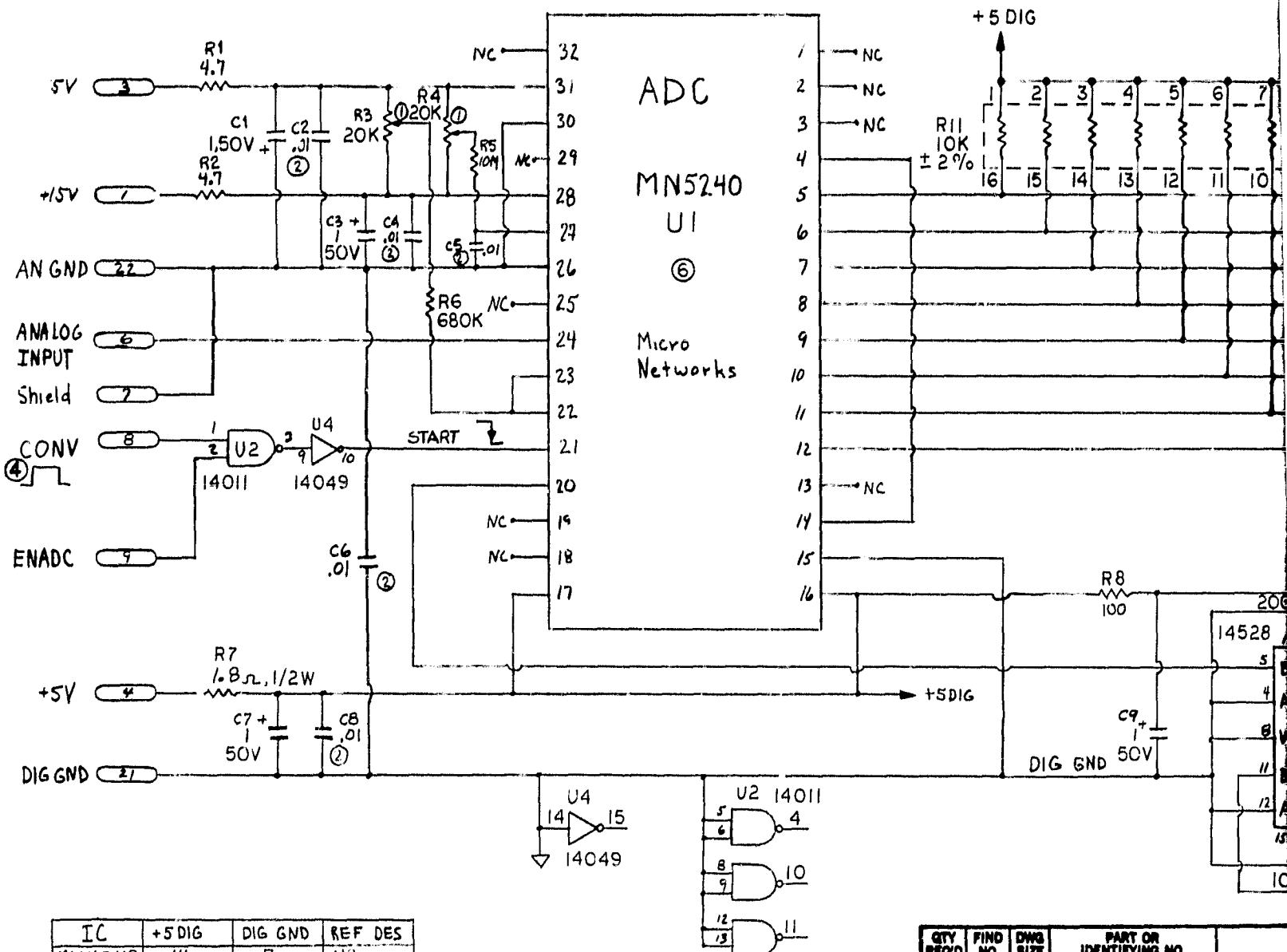
SCHEMATIC DIAGRAM
CAMERA MICROCONTROLLER BD. "J"
27.074 CCD CAMERA

SIZE	CODE IDENT NO.		REV
C	21802	652-4102	—
SCALE			SHEET

FOLDOUT FRAME

5 SEE LAYOUT CONSIDERATION MN5240 DATA SHEET.

⑥ ADC MOUNTED IN A MANNER . MILAR TO THE TMS2516 ON THE MEMOR. BOARD.



IC	+5 DIG	DIG GND	REF DES
MC14011B	14	7	U2
MC14049UB	1	8	U3, U4

QTY REQ'D	FIND NO.	DWG SIZE	PART OR IDENTIFYING NO.

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES.
TOLERANCE ON
DECIMALS: .XX ± .XXX ± FRAC ± ANGLES ±
CONCENTRICITY .005 TIR
REMOVE BURRS & SHARP EDGES
ALL MACHINED SURFACES 125 √
DO NOT SCALE THIS DRAWING
MATERIAL
FINISH

CONTRACT NO.
DRAWN S. Count
CHECK m a %
MFG
ENGR MECH
PROJECT ENGR
ADDNL APPD

NEXT ASSY | USED ON
APPLICATION

BRUNING 44-232-30433-9

FOLDOUT FRAME

E LAYOUT CONSIDERATION MN5240 DATA SHEET.

C MOUNTED IN A MANNER SIMILAR TO
E TMS2516 ON THE MEMORY BOARD.

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

F. I. ALITY

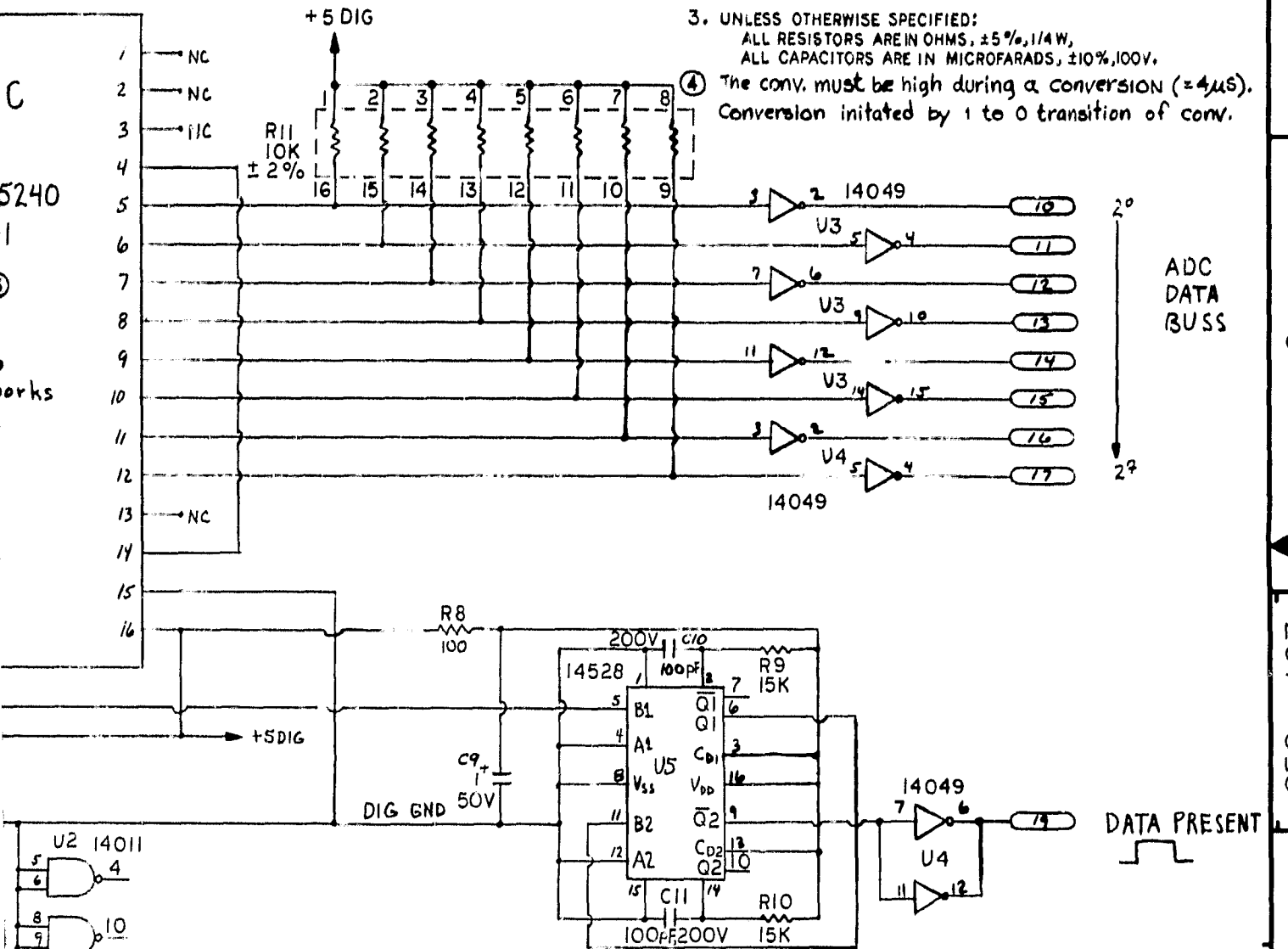
Notes:

① Use 10 turn pots value from 10K to 100K
BOURNS 3059P 20K MOUNT NEAR END OF THE BOARD.

② Locate close to the MN 5240

3. UNLESS OTHERWISE SPECIFIED:
ALL RESISTORS ARE IN OHMS, ±5%, 1/4 W,
ALL CAPACITORS ARE IN MICROFARADS, ±10%, 100V.

④ The conv. must be high during a conversion (≈4μs).
Conversion initated by 1 to 0 transition of conv.



652-4103

QTY REQ'D	FIND NO.	DWG SIZE	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	NOTE

PARTS LIST

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES.
TOLERANCE ON
DECIMALS XX ± XXX ± FRAC ± ANGLES ±
CONCENTRICITY .005 TIR
REMOVE BURRS & SHARP EDGES
ALL MACHINED SURFACES 125 ✓
DO NOT SCALE THIS DRAWING
MATERIAL
FINISH
NEXT ASSY | USED ON
APPLICATION

CONTRACT NO.

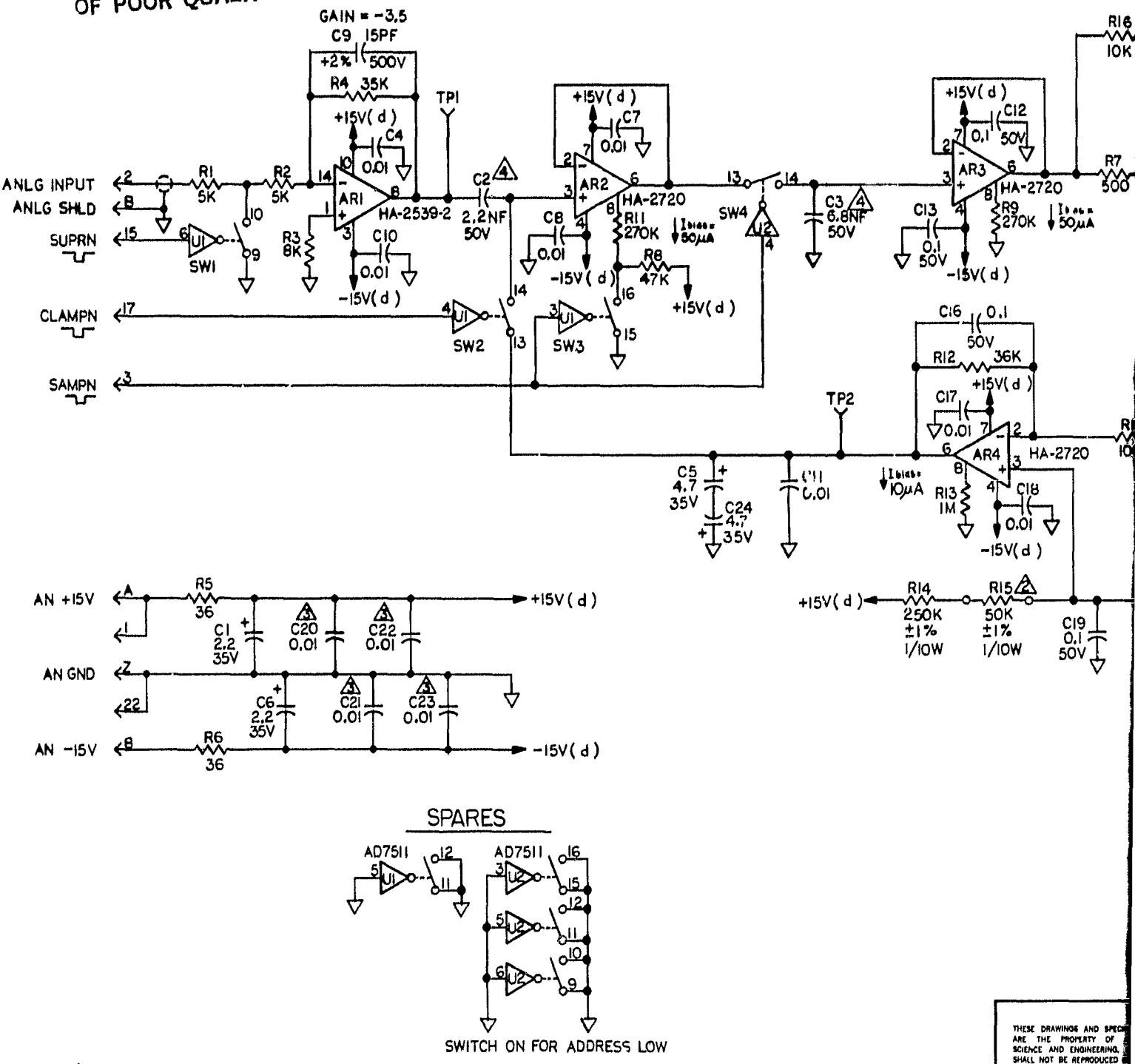
DRAWN	R. Counterman	4/24/84
CHECK	m a Vmonelli	11/26/84
MFG		
ENGR MECH	ENGR ELEC R. Counterman	
PROJECT ENGR	QUAL ASSUR	
ADDNL APPD		

AMERICAN SCIENCE AND ENGINEERING
CAMBRIDGE, MASS.

SCHEMATIC DIAGRAM
ADC BOARD I, 27.074 CCD CAMERA

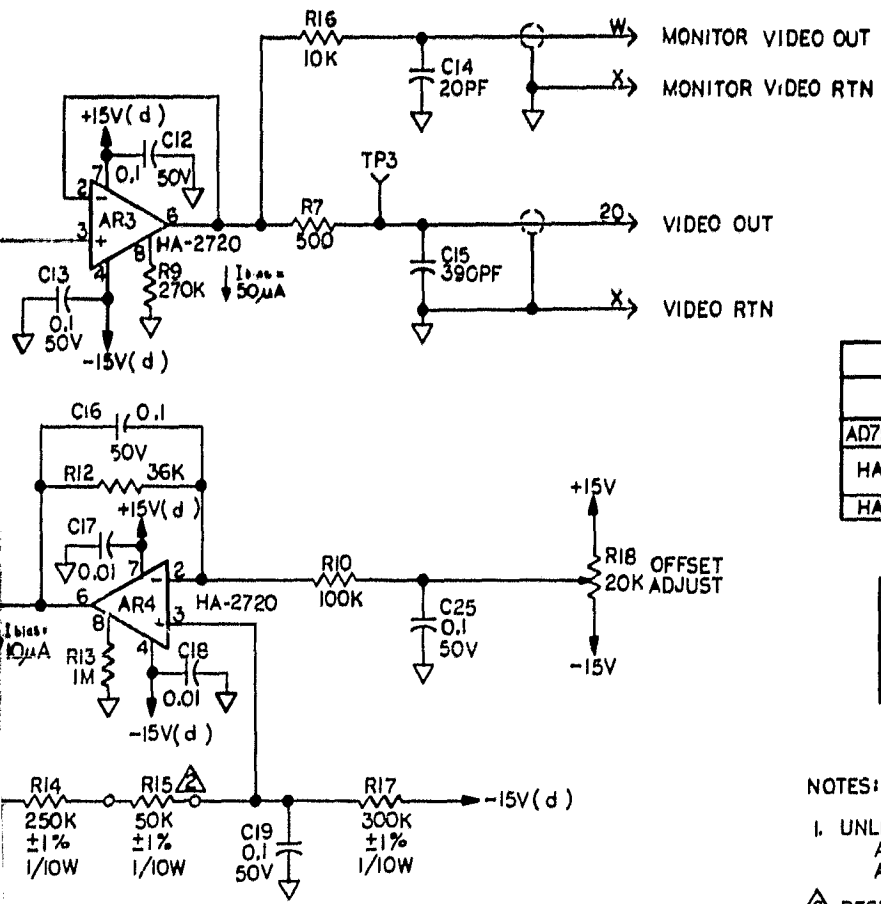
SIZE	CODE IDENT NO.		REV
C	21802	652-4103	—
SCALE NONE			SHEET 1 OF 1

FOLDOUT FRAME



FOLDOUT FRAME

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



POWER DISTRIBUTION TABLE					
IC	+15V(d) PIN NO.	-15V(d) PIN NO.	RTN PIN NO.	REF DES	PINS NOT USED
AD7511DISD	8	1	2	U1, U2	
HA-2539-2	10	3		AR1	2,4-7 9,11-13
HA-2720	7	4		AR2, AR3, AR4	1, 5

HIGHEST REF DES USED							
AR3	C25	R18	TP3	U2			
REF DES NOT USED							

CAP TABLE (4)	
REF DES	USED WITH
C20, C21	U1
C22, C23	U2

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   ALL CAPACITANCE VALUES ARE IN MICROFARAD, ±10%, 100V
   ALL RESISTANCE VALUES ARE IN OHMS, ±5%, 1/4W

(2) RESISTOR VALUE IS NOMINAL, ACTUAL VALUE IS TO BE DETERMINED AT TEST.

(3) CAPACITORS ARE TO BE LOCATED AS CLOSE AS POSSIBLE TO THEIR RELATED IC'S.

(4) C2 & C3 ARE METALIZED POLYCARBONATE CAPACITORS PURCHASED FROM: S&EI MFG. CAPS NORTHRIDGE, CA.
P/N 9-22EIA222K-C2
P/N 9-22EIA682K-C3

5. (ESD) AD7511DISD IS AN ELECTROSTATIC DEVICE AND MUST BE HANDLED PER THE REQUIREMENTS OF AS&E 500-9000.

FOLDOUT FRAME

652-4104

QTY REQ'D	FIND NO.	DWG SIZE	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	NOTE

PARTS LIST

INTERPRET THIS DRAWING IN ACCORDANCE WITH DOD-STD-100

NEXT ASSY | USED ON

APPLICATION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES. TOLERANCE ON
DECIMALS .XX ± — .XXX ± — FRAC ± — ANGLES ± —
CONCENTRICITY .005 TIR
REMOVE BURRS & SHARP EDGES
ALL MACHINED SURFACES 125 ✓
DO NOT SCALE THIS DRAWING
MATERIAL
FINISH

CONTRACT NO.

DRAWN	Gomez	10-31-84
CHECK		
MFG		
ENGR MECH	ENGR ELEC	
PROJECT ENGR	QUAL ASSUR	
ADDNL APPD		

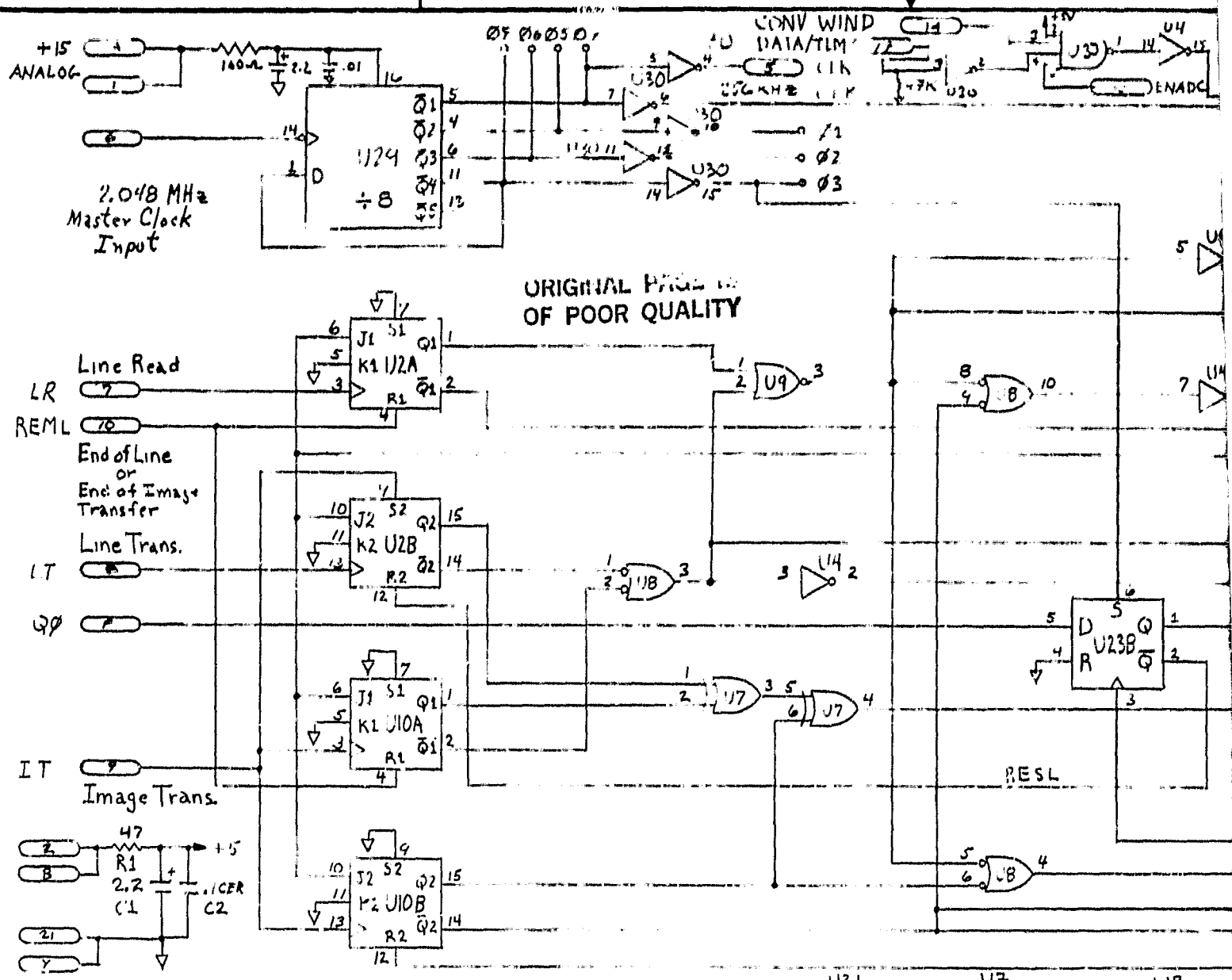
AMERICAN SCIENCE AND ENGINEERING
CAMBRIDGE, MASS.

SCHEMATIC
CORRELATED DBL SAMPLE/HOLD BD H
27,074 CCD CAMERA

SIZE	CODE IDENT NO.	
D	21802	652-4104

REV —

SCALE NONE | SHEET 1 OF 1



IC	+15	GND	REF DES
MC14018B	16	2378	U29
—	—	4 10 12 15	U29
MC14027B	16	8	U2 U10
MC14049B	1	8	U30 U4
MC14520B	16	8	U5
MC14050B	1	8	U31
MC14070B	14	7	U7
MC14011B	14	7	U8
MC14001B	14	7	U9
MC14013B	14	7	U23B U32
MC14012B	14	7	U33

FOLDOUT FRAME

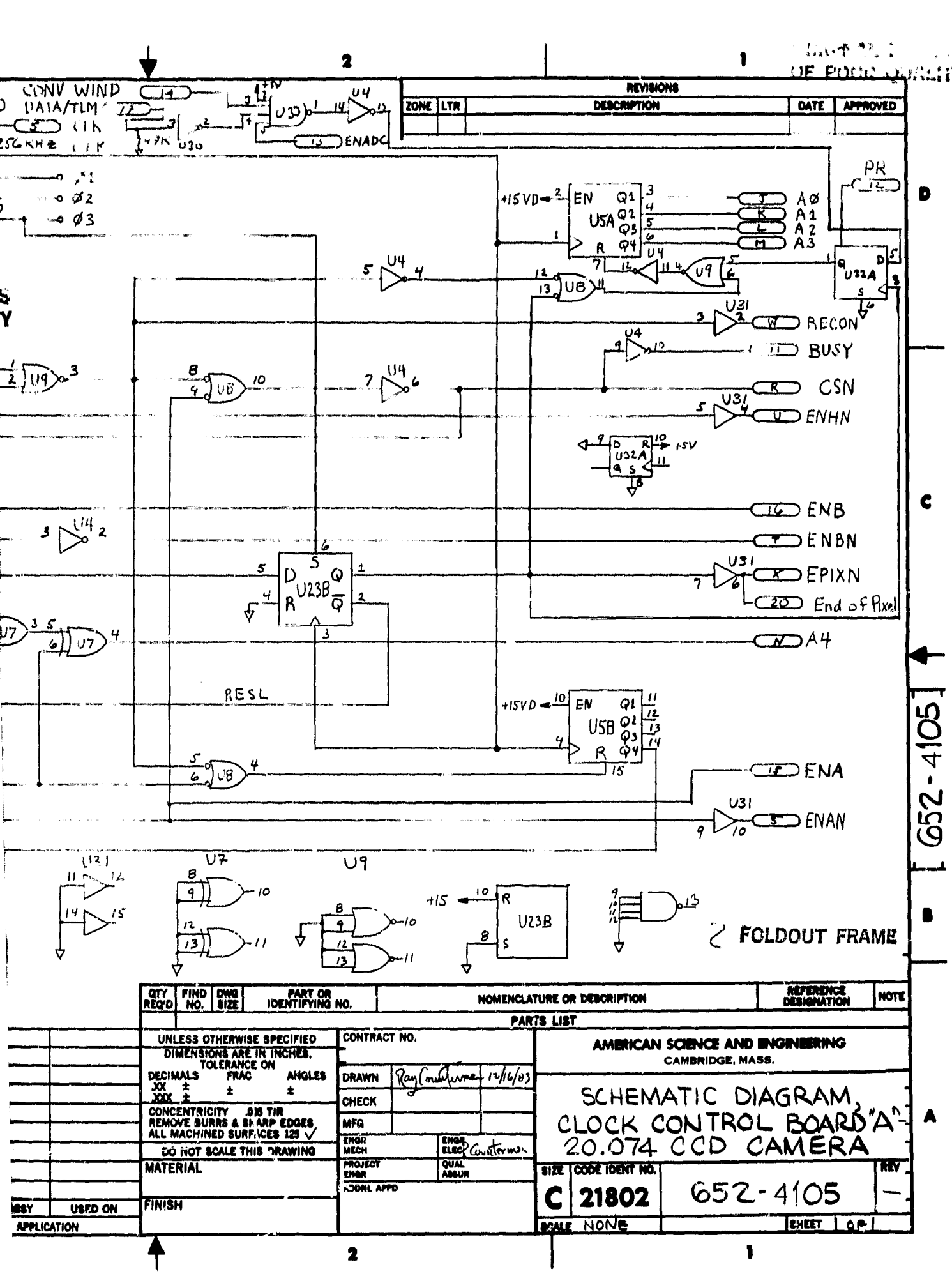
QTY REQ'D	FIND NO.	DWG SIZE	PART OR IDENTIFYING NO.

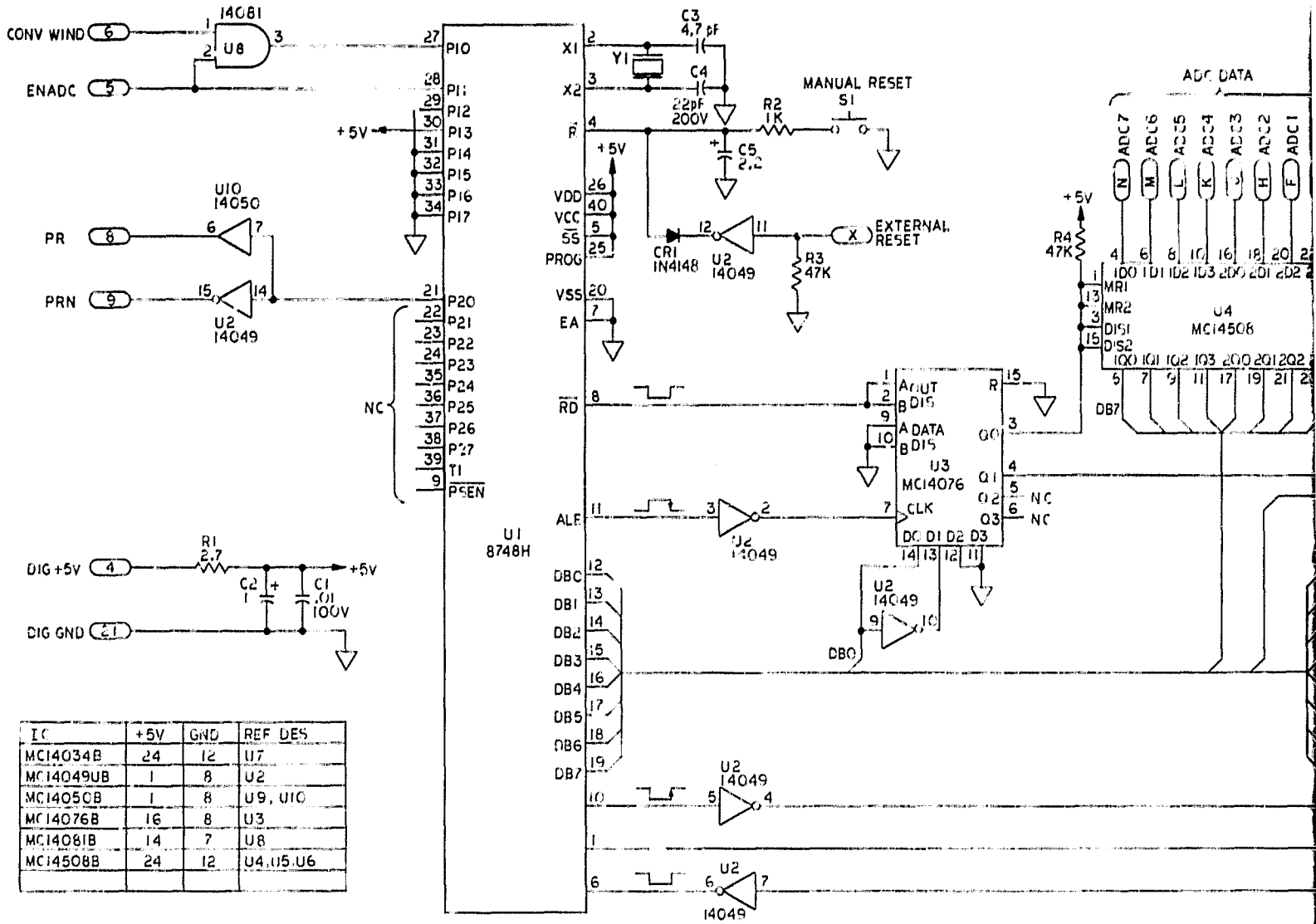
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES.
TOLERANCE ON
DECIMALS FRAC ANGLES
XX ± ± ±
XXX ±
CONCENTRICITY .005 TIR
REMOVE BURRS & SHARP EDGES
ALL MACHINED SURFACES 125 √
DO NOT SCALE THIS DRAWING
MATERIAL
FINISH

CONTRACT NO
DRAWN
CHECK
MFG
ENGR
MECH
PROJECT ENGR
ADDNL APPD

NEXT ASSY | USED ON
APPLICATION

BRUNING 44 232 30433 9

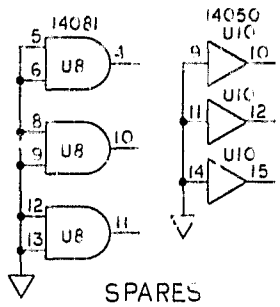

REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
CONV WIND
DATA/TLM
CLK
256KHz CLK
ENADC
+15VD
U5A
U5B
U23B
U32A
U31
U4
U7
U8
U9
U12
PR
A0
A1
A2
A3
RECON
BUSY
CSN
ENHN
ENB
ENBN
EPIXN
End of Pixel
A4
RESL
ENA
ENAN
+5V
+15
FOLDOUT FRAME
652-4105
QTY REQ'D | FIND NO. | DWG SIZE | PART OR IDENTIFYING NO. | NOMENCLATURE OR DESCRIPTION | REFERENCE DESIGNATION | NOTE
PARTS LIST
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES.
TOLERANCE ON
DECIMALS FRAC ANGLES
XX ± ± ±
XXX ±
CONCENTRICITY .005 TIR
REMOVE BURRS & SHARP EDGES
ALL MACHINED SURFACES 125
DO NOT SCALE THIS DRAWING
MATERIAL
FINISH
USED ON
APPLICATION
CONTRACT NO.
DRAWN
CHECK
MFG
ENGR MECH
ENGR ELEC
PROJECT ENGR
QUAL ASSUR
ADDNL APPD
AMERICAN SCIENCE AND ENGINEERING
CAMBRIDGE, MASS.
SCHEMATIC DIAGRAM,
CLOCK CONTROL BOARD "A"
20.074 CCD CAMERA
SIZE
C
CODE IDENT NO.
21802
652-4105
REV
—
SCALE NONE
SHEET



IC	+5V	GND	REF DES
MC14034B	24	12	U7
MC14049UB	1	8	U2
MC14050B	1	8	U9, U10
MC14076B	16	8	U3
MC14081B	14	7	U8
MC14508B	24	12	U4,U5,U6

NOTES:

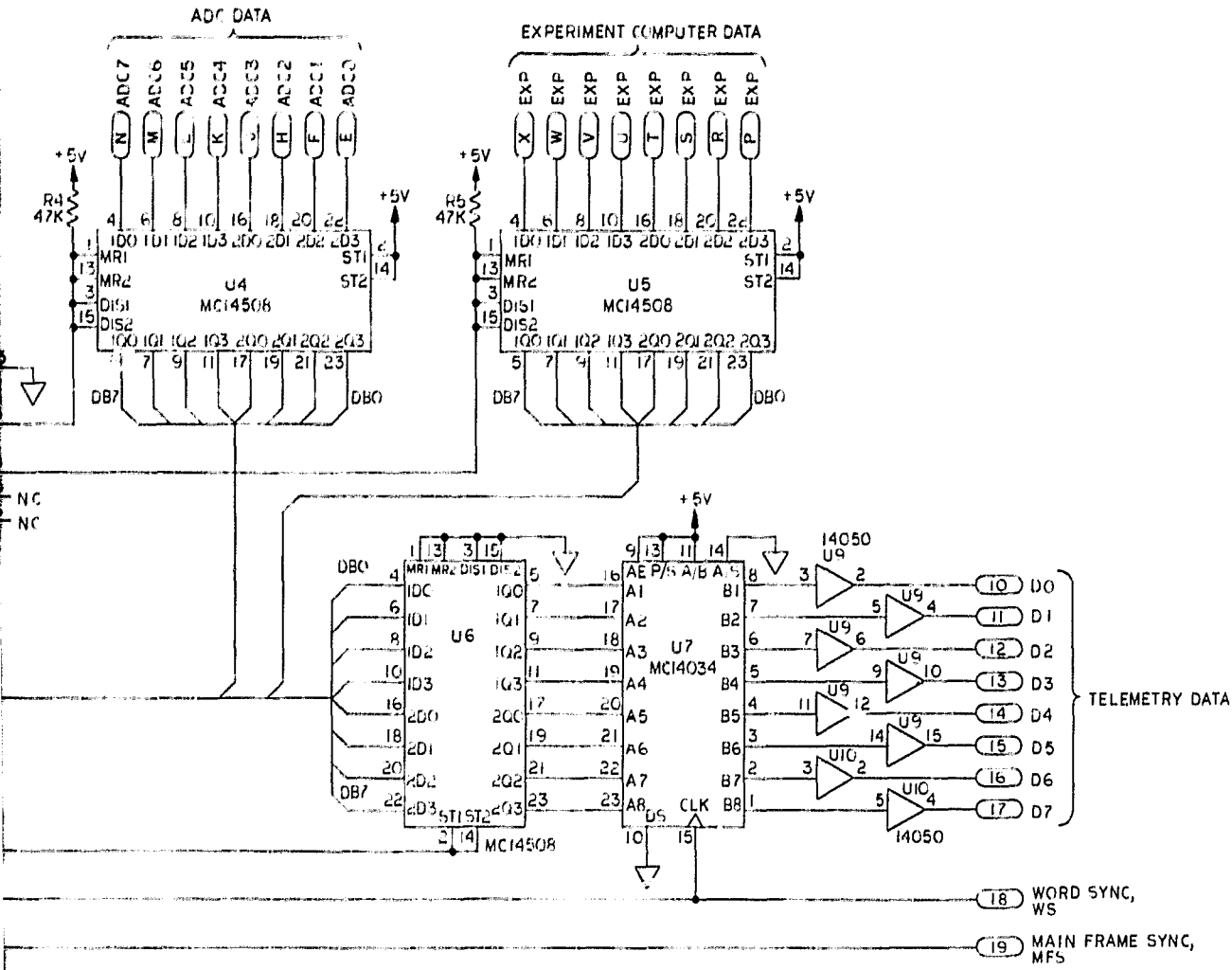
1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTOR VALUES ARE IN OHMS, ±5%, 1/4W;
   ALL CAPACITOR VALUES ARE IN MICROFARADS, ±10%, 50V.



DRAWING 44232 30433 9

FOLDOUT FRAME

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



QTY REQ'D	FIND NO.	DWG SIZE	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	NOTE
			PARTS LIST			

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INTERPRET THIS DRAWING IN ACCORDANCE WITH DOD STD 100

NEXT ASSY | USED ON

APPLICATION

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES, TOLERANCE ON
DECIMALS XX ± . XXX ± . FRAC ± ANGLES ±
CONCENTRICITY .005 TIR
REMOVE BURRS & SHARP EDGES
ALL MACHINED SURFACES 125 ✓
DO NOT SCALE THIS DRAWING
MATERIAL
FINISH

CONTRACT NO.

DRAWN	R FAINBERSH	11/21/84
CHECK		
MFG		
ENGR MECH	ENGR ELEC	
PROJECT ENGR	QUAL ASSUR	
ADDNL APPD		

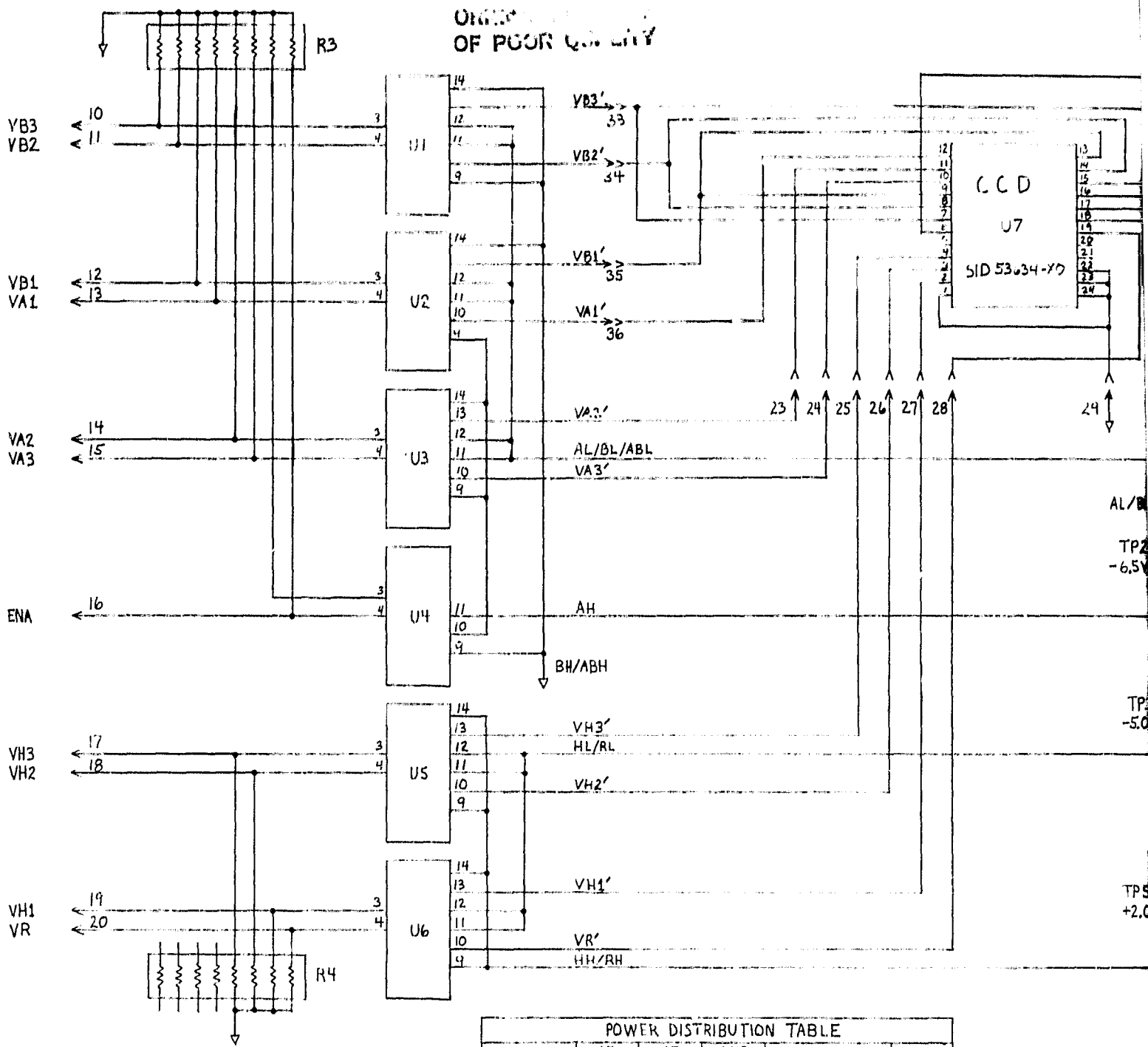
AMERICAN SCIENCE AND ENGINEERING
CAMBRIDGE, MASS.

SCHEMATIC DIAGRAM
TELEMETRY MICROCONTROLLER
BOARD K, 27.074 CCD CAMERA

SIZE	CODE IDENT NO.		REV
D	21802	652-4106	-
SCALE NONE		SHEET 1 OF 1	

652-4106

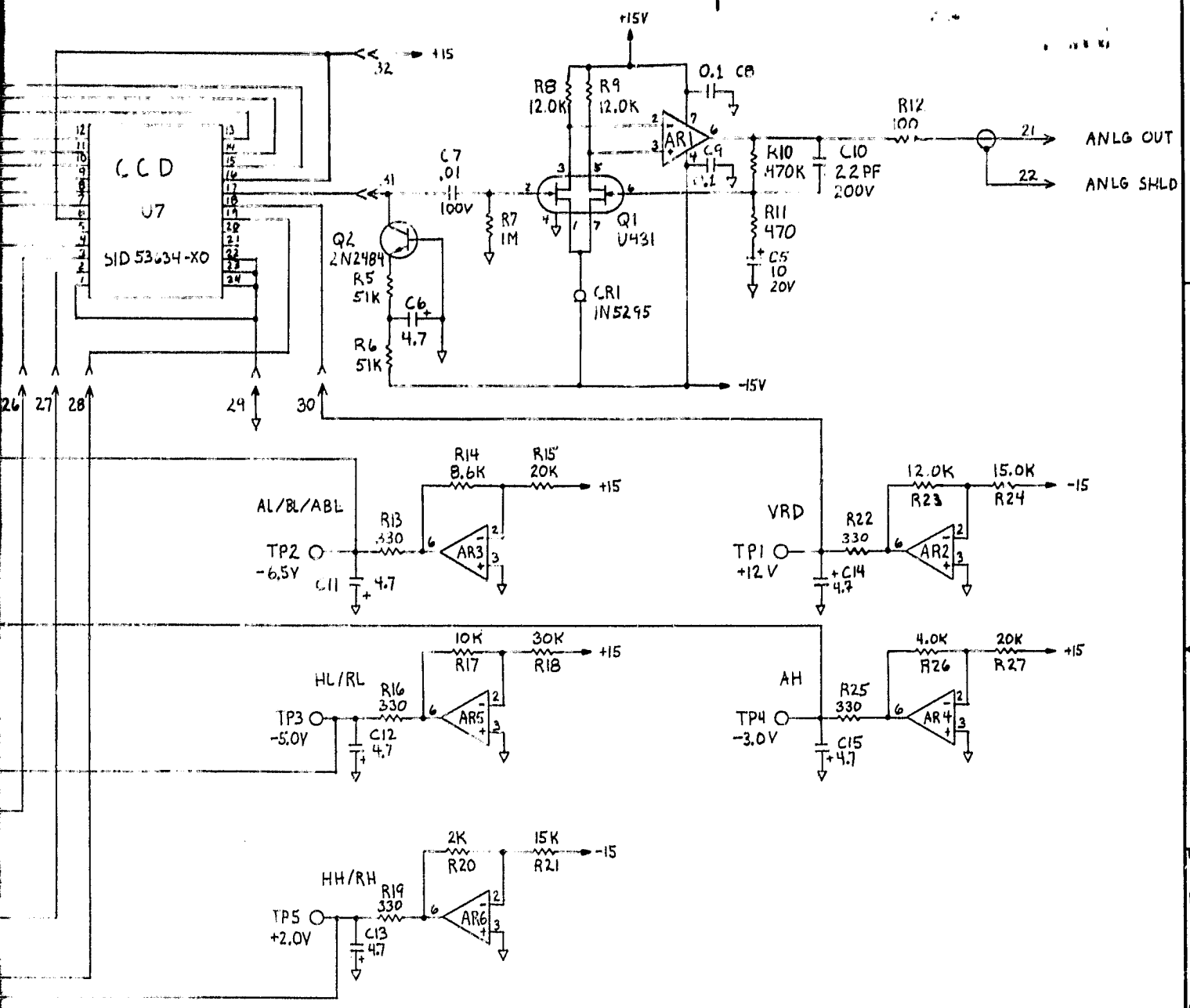
FOLDOUT FRAME



POWER DISTRIBUTION TABLE					
IC	+15 PIN NO.	-15 PIN NO.	GND PIN NO.	REF DES	PINS NOT USED
AD7512DISD	7	1	2	U1 - U6	5,6,8
AD741LN	7	4		AR2 - AR6	5,8
MP5501HY	7	4		AR1	

NOTES
1. UNLESS OTHERWISE SPECIFIED
   ALL RESISTANCE VALUES ARE IN OHMS, ±5%, ¼W
   ALL CAPACITANCE VALUES ARE IN MICROFARAD, ±10%, 50V
2. U7 IS NOT MOUNTED ON THIS PC BOARD

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED



652-4107

PINS NOT USED
5,6,8
5,8

±5%, 1/4W
ARAD, ±10%, 50V
RD

QTY REQ'D	FIND NO.	DWG SIZE	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	REFERENCE DESIGNATION	NOTE

PARTS LIST

NEXT ASSY	USED ON
APPLICATION	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES, TOLERANCE ON
DECIMALS XX ± XXX ± FRAC ± ANGLES ±
CONCENTRICITY .005 TIR
REMOVE BURRS & SHARP EDGES, ALL MACHINED SURFACES 125 ✓
DO NOT SCALE THIS DRAWING
MATERIAL
FINISH

CONTRACT NO.

DRAWN	R Counterman	11/28/84
CHECK		
MFG		
ENGR MECH	ENGR, ELEC	R Counterman
PROJECT ENGR	QUAL ASSUR	
ADDNL APPD		

AMERICAN SCIENCE AND ENGINEERING
CAMBRIDGE, MASS.

SCHEMATIC DIAGRAM
CCD HEAD ELECTRONICS
27.07a CCD CAMERA

SIZE	CODE IDENT NO.		REV
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SCALE		SHEET 1 OF 1	

FOLDOUT FRAME